ISSN: 2321-7782 (Online)
e-ISJN: A4372-3114
Impact Factor: 7.327

Volume 6, Issue 4, April 2018

International Journal of Advance Research in Computer Science and Management Studies

Research Article / Survey Paper / Case Study

Available online at: www.ijarcsms.com

Design and Implementation of Adaptive LMS Filtering Algorithm for Noise Cancellation on FPGA

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Abstract: ***Lately FPGA frameworks are supplanting committed Programmable Digital Signal Processor (PDSP) frameworks because of their more noteworthy adaptability and higher transmission capacity, coming about because of their parallel structural planning. This paper introduces the materialness of a FPGA framework for discourse transforming. Here versatile separating system is utilized for clamor retraction in discourse signal. Minimum Mean Squares (LMS) , one of the generally utilized calculation as a part of numerous sign handling environment , is actualized for adaption of the channel coefficients. The retraction framework is executed in VHDL also tried for clamor wiping out in discourse signal. The recreation of VHDL outline of versatile channel is performed and broke down on the premise of Signal to Commotion degree (SNR) and Mean Square Error (MSE).***

Keywords: Adaptive Filter, LMS Algorithm, Active Noise cancellation, VHDL Design, SNR, MSE.

I. INTRODUCTION

The computerized sign handling applications force impressive compels on range, power scattering, speed and expense. In this way the outline apparatus ought to be precisely picked. The most widely recognized apparatuses for the outline of such application are ASIC, DSP and FPGA. The DSP utilized for to a great degree complex math-serious errands yet can't transform high testing rate applications because of its serial structural planning. Though ASIC confronts absence of adaptability also oblige long outline cycle. The FPGA (Field programmable Gate Array) can make up drawbacks of ASIC and DSP. Thus FPGA has turned into the best decision for the outline of sign preparing framework because of their more noteworthy adaptability and higher transfer speed, coming about from their parallel structural engineering.

This paper explores the materialness of a FPGA framework for continuous sound transforming frameworks. In late years, acoustic commotions get to be more clear due to boundless utilization of modern gears. An Active (additionally called as Adaptive) clamor retraction (ANC) is a strategy that viably constricts low frequencies undesirable commotion where as latent strategies are either insufficient or has a tendency to be exceptionally extravagant or massive. An ANC framework is focused around a ruinous obstruction of a hostile to clamor, which have level with abundancy and inverse stage copy of essential undesirable commotion. Emulating the superposition standard, the result is commotion free unique sound.

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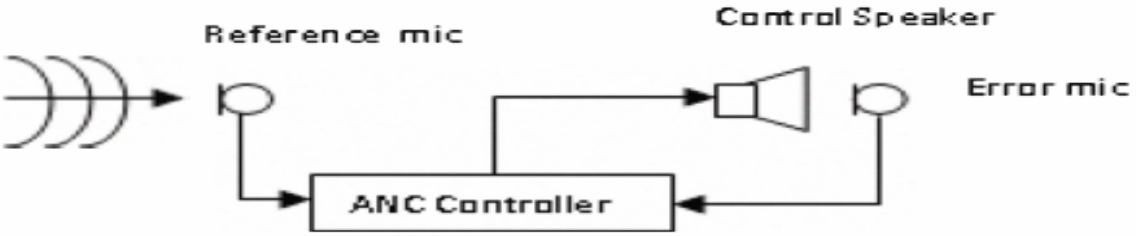

Figure 1. Basic concept of ANC

ANC systems are distinguished by their different goals that lead to different architectures. If all ambient sound shall be reduced, a feedback system with its simpler architecture may be used. If, as in our case, single sources of unwanted sound shall be compensated, a feed forward system is required. A feed forward system as shown in fig. 1 is characterized by two audio inputs per channel: one reference signal input for the sound to be removed, and second error input for the sound after the compensation.

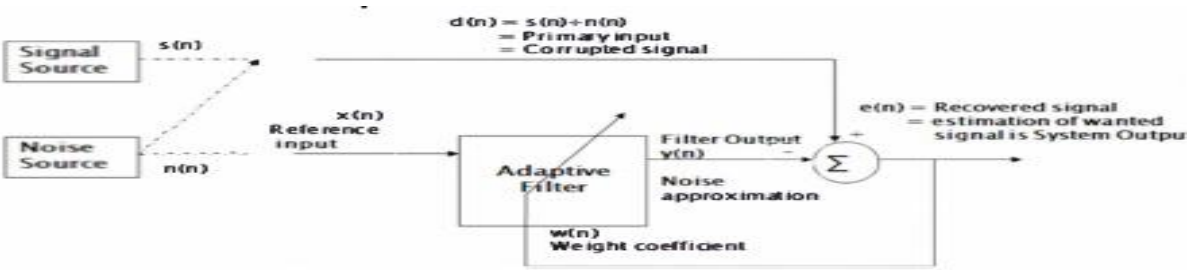

Figure 2. Adaptive Noise Canceller

A versatile FIR encourage forward framework is appeared straightforward route in fig 2. For the particular retraction of irritating clamor without influencing different sounds. [2] It is double enter framework. The principal inputs is essential sign sanctum) which is needed sign (say s(n)) ruined by clamor (say n(n)). The second include is reference signal x(n) can be interfacing clamor expected to be uncorre1ated with the needed flag however corresponded with commotion influencing unique flag in an obscure way. The channel yield sign yen) is an assessment of the clamor signal with altered sign. This sign and the essential sign are superposed, with the goal that the commotion sign is scratched off and blunder signal e(n) is the aftereffect of this superposition which constitutes the general framework yield. The versatile separating operation attained the best comes about when framework yield is commotion free. This objective is attained by minimizing the mean square of the slip signal [3]. The generally favored LMS calculation is utilized for the adaption of the channel coefficients.

A. Mathematical treatment

Consider the transversal channel with data x(n) i.e. vector of the M(filter length) latest information tests at examining point n.

$$x(n) = [x(n), x(n-1), \ldots x(n-M+1)] \quad (1)$$

and w(n) i.e. vector of filter coefficients as

$$w(n) = [w_0(n), w_1(n), \ldots w_{M-1}(n)] \quad (2)$$

At some discrete time n, the filter produces an output yen) which is linear convolution sum given by

$$y(n) = \sum_{k=0}^{M-1} w(n)\ x(n-k) \quad (3)$$

Also can be represent in vector form as

$$y(n) = w^T(n)\, u(n) \qquad (4)$$

The error signal is difference of this output with the Primary signal den) given by,

$$e(n) = d(n) - y(n) \qquad (5)$$

And by squaring error we get

$$e^2(n) = d^2(n) - 2d(n)x^T(n)w(n) + w^T(n)x(n)x^T(n)w(n) \qquad (6)$$

To optimize the filter design, we choose to minimize the mean-square value of e(n). Thus the cost function is defined as the MSE denoted by J

$$J = E[e(n)e^*(n)] = E[|e(n)|^2] \qquad (7)$$

Where E denotes the statistical expectation operator.

Applying the operator V to the cost function J, a gradient vector V J obtain as

$$\nabla J(n) = -2P + 2Rw(n) = -2x(n)d(n) + 2x(n)x^T(n)w(n) \qquad (8)$$

Where, R is the autocorrelation matrix of x(n), and P is the cross correlation matrix of den) and x(n).

The LMS calculation is focused around steepest-drop system. To form steepest-plunge system, consider an expense capacity J(w) i.e. a persistently differentiable capacity of some obscure weight vector w.

To find an optimal solution Wo (initial guess) that satisfies the condition

$$J(w_0) \le J(w) \quad \text{for all } w \qquad (9)$$

Which is a mathematical statement of unconstrained optimization.

Beginning with w(o), produce a succession of weight vector w(1), w(2), ... ,such that the expense capacity J(w) is decreased at every cycle of the calculation. in this way

$$J(w(n+1)) < J(w(n)) \qquad (10)$$

Where w(n) is the old value of the weight vector and

w(n+ 1) is its updated value Substituting the estimate of equation (8) for the gradient vector V' J (n)

The steepest-descent algorithm, a new recursive relation obtain for updating the weight vector as

$$w(n+1) = w(n) + \mu x(n)e(n) \qquad (11)$$

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A scaling component 1.1 presented here is step size parameter used to control the step width of the cycle what's more therefore the dependability and joining velocity of the calculation [4,5].

The LMS algorithm is convergent in mean square if and only if 1.1 satisfies the condition.

$$0 < \mu < \frac{1}{(M \times \overline{P})} \qquad (12)$$

II. VHDL Implementation of System

The VHDL design of the system is as shown in Fig. 3. Arithmetic is modeled with Q format number representation which provides for each pipeline stage an appropriate number of guard bits for representing the integer part and avoiding overflow effects.

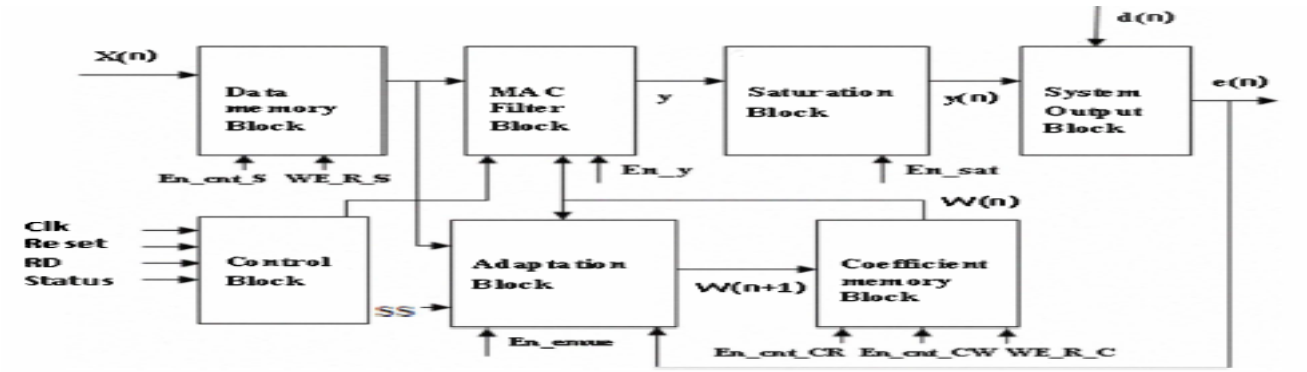

Figure 3. VLSI Design of the adaptive filter

The design splits into seven blocks as follows:

1. *Data Memory block:* The single port RAM is designed for storage of the audio samples.

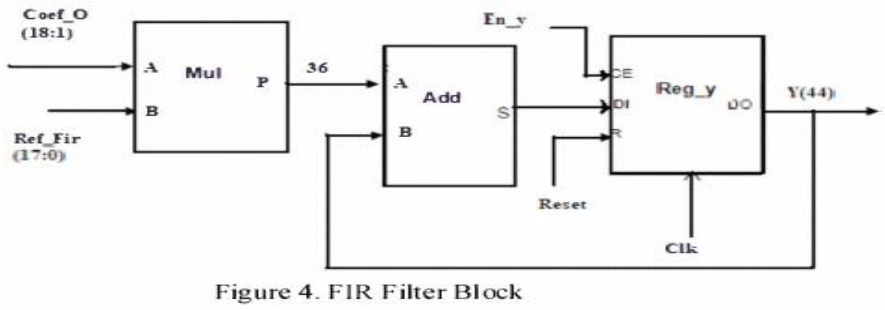

Figure 4. FIR Filter Block

Most extreme information way length short, the channel is actualized as a consecutive MAC unit which performs M gatherings of items amid each example period so that an asset imparting can be used. since the sound example period fs gives a lot of accessible clock cycles for every sound example, no parallel structure with M multipliers and M-1 adders is important. This piece is outlined as three-stage pipeline for the separating cycle The information tests read from the information RAM square are increased with their relating channel coefficient taken from the double ported Coefficient RAM square what's more put away in the collector.

2. *Saturation Block:* The channel yield sign is encouraged to the immersion piece, which keeps the channel yield from flood and rearranges the indication of the yield sign to give the stage movement to the recompense step.

3. *System output block:* The Adder unit is utilized to execute mathematical statement of mistake sign e(n) from immersion square yield y(n) and essential sign sanctum. This yield is the obliged framework yield.

4. *Adaption Block algorithm:* A four-stage pipeline structure intended for the adjustment of the coefficients. The coefficient is figured by a result of the data test (Recfir), the slip sign (Err) and Step size parameter (SS). A register is

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embedded to this way that parts the number-crunching chain for attaining a shorter signal defer so a clock recurrence of felk = 50mhz can be met.

5. *Coefficients Memory block:* This block designed for storage of the current filter coefficients. The dual port RAM is chosen to support a parallel processing of the coefficient update block and the FIR Filter block. With two address inputs the reading address of the coefficients and the address for writing back the updated coefficients can be incremented within two interleaved clock periods.

6. *Control Block:* The Control way usefulness is actualized as the Finite state machine (FSM). The FSM controls the handling of the two parallel pipelined information ways. The state chart of the FSM indicated in fig. 6 portrays

7. *MAC Filter Block:* The FIR channel outline is taking into account the transposed immediate structure to keep the sequence which is started with each new input sample pair Err (error signal) and XN (reference signal). Total seven states are specified.

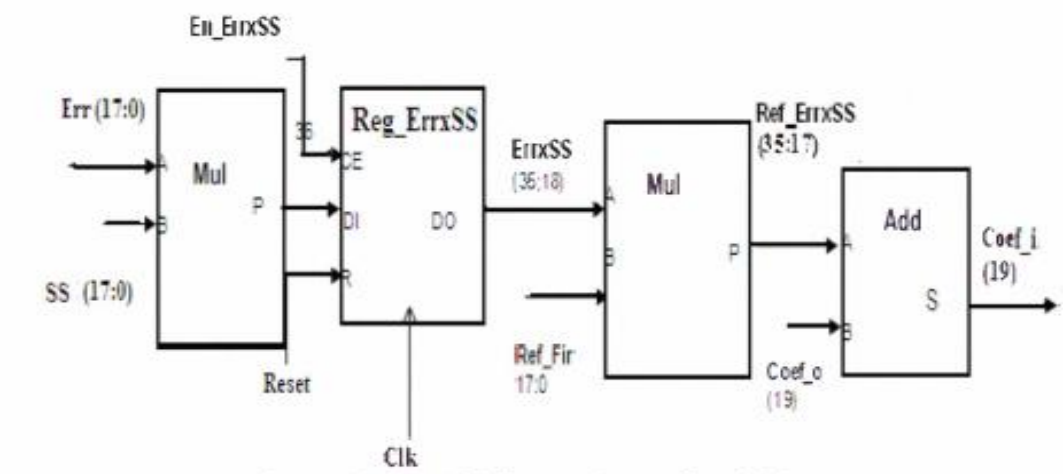

Figure 5. Coefficient Adaptation Unit

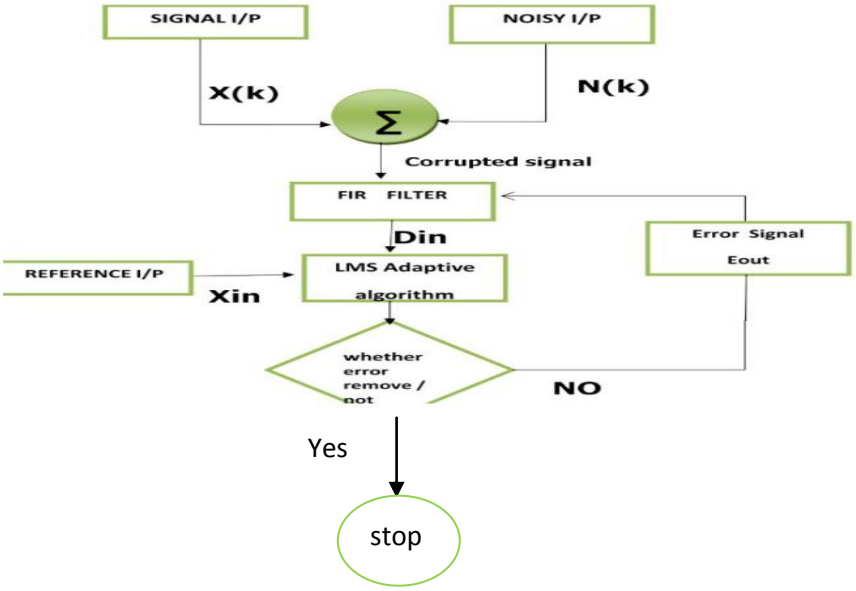

Figure 6. Design flow chart

III. Simulation and Results

Xilinx ISE 13.2 improvement environment was utilized for usage of above VLSI outline. The configuration has been exchanged to VHDL code and its the fittings reenactment finished with the Xilinx ISE test system furthermore executed on Spartan-3 FPGA Xc3s400pq208-5 board.

The sound is taken as wave record for testing of framework. A direct blend of the produced commotion and the unique sign is utilized as the essential information for the channel. The ref. sign is commotion which is corresponded variant of commotion included with unique sign Channel yield is recompense sign meant by yet) which is clamor estimate. The framework yield is lapse signal meant by e(t) which is recuperated sign. The Q17 configuration is utilized for math processing's. The figure 7 and 8 shows combination report and RTL (Register-exchange level) schematic of composed framework separately. The FPGA use reported is beneath 68% for all asset classifications for channel request of 256 .Just 3 of the 16 accessible installed multipliers were utilized and the transposed immediate structure FIR channel contains stand out multiplier and one snake paying little respect to the channel request. The longest information way in the framework is given by the increase include operations of the coefficient adaption and limits the clock recurrence got up to 80mhz.

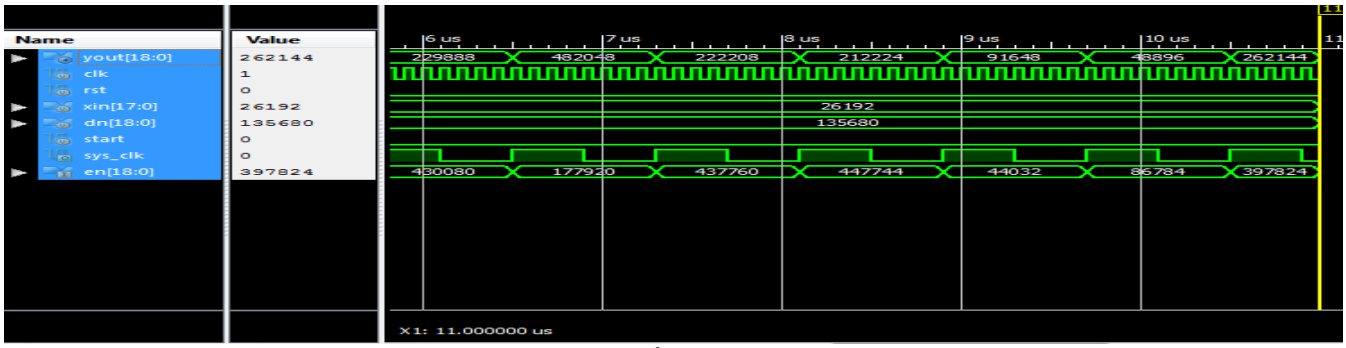

Fig. 7 combination report

Timing Report

Speed Grade: -4

Minimum period: 25.759ns (Maximum Frequency: 38.821MHz)

Minimum input arrival time before clock: 26.443ns

Maximum output required time after clock: 6.686ns

Maximum combinational path delay: No path found

Timing Detail:

All values displayed in nanoseconds (ns)

==========

Timing constraint: Default period analysis for Clock 'AD/sys_clk1'

Clock period: 25.759ns (frequency: 38.821MHz)

Total number of paths / destination ports: 1512555 / 35

Area Report

Selected Device : 3s500efg320-4

Number of Slices : 117 out of 4656 2%

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Number of Slice Flip Flops : 46 out of 9312 0%

Number of 4 input LUTs : 222 out of 9312 2%

Number of IOs : 59

Number of bonded IOBs : 59 out of 232 25%

Number of MULT18X18SIOs : 4 out of 20 20%

Number of GCLKs : 2 out of 24 8%

HDL Synthesis Report

Macro Statistics

ROMs : 1

16x18-bit ROM : 1

Multipliers : 2

18x18-bit multiplier : 1

19x18-bit multiplier : 1

Adders/Subtractions : 2

18-bit adder : 1

19-bit adder : 1

Counters : 2

13-bit up counter : 1

4-bit up counter : 1

Registers : 3

1-bit register : 2

19-bit register : 1

Latches : 7

1-bit latch : 7

Comparators : 1

4-bit comparator greater : 1

Xors : 19

1-bit xor2 : 1

1-bit xor3 : 18

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==========* Advanced HDL Synthesis *

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Analyzing FSM <FSM_0> for best encoding.

Optimizing FSM <CB/ps/FSM> on signal <ps[1:6]> with one-hot encoding.

State | Encoding

---

000 | 000001

001 | 000010

010 | 000100

011 | 001000

100 | 010000

101 | 100000

110 | unreached

==========Advanced HDL Synthesis Report

Macro Statistics

# FSMs	:	1
# ROMs	:	1
16x18-bit ROM	:	1
# Multipliers	:	2
18x18-bit multiplier	:	1
19x18-bit multiplier	:	1
# Adders/Subtractors	:	2
18-bit adder	:	1
19-bit adder	:	1
# Counters	:	2
13-bit up counter	:	1
4-bit up counter	:	1
# Registers	:	21
Flip-Flops	:	21
# Latches	:	7
1-bit latch	:	7
# Comparators	:	1

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4-bit comparator greater	:	1
# Xors	:	19
1-bit xor2	:	1
1-bit xor3	:	18

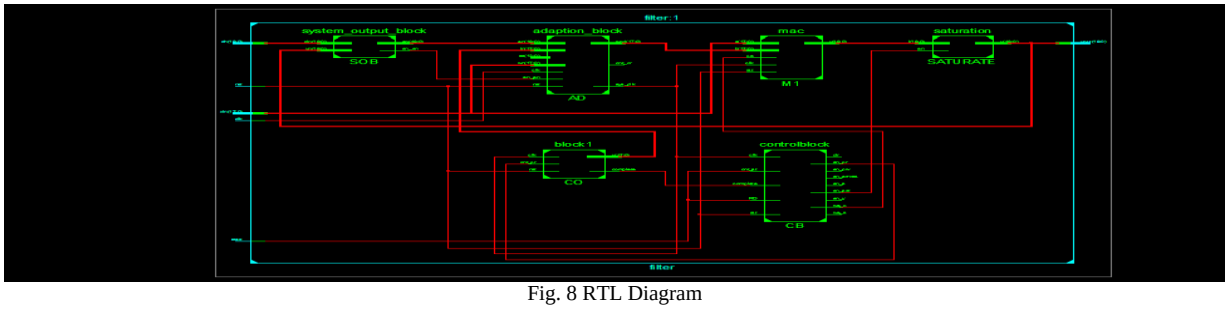

Fig. 8 RTL Diagram

IV. Conclusion

The FPGA platform is well suited for the complex real time audio processing. An adaptive noise cancellation process has successfully been implemented. When tested with different signals, the system showed an improved performance compared to the original signal. For future work, we planned to implement this system with AFA (Adaptive Filtering with Averaging) algorithm which converge rapidly with lower complexity.

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