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Forward Error Correcting Implementation using Convolution Encoder and Viterbi Decoding

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Abstract: : *Viterbi decoder is employed in wireless communication to decode the convolution codes ;those codes are used in or every robust digital communication system .Convolution encoding and veterbi decoding is a powerful method f or error correction this paper deals with synthesis ands and implementation of veterbi decoder with aconstraint lenth three and code rate 1/2 and 1/3 in FPGA (field programmable gate array) The performance of veterbi decoder is se init erms of recourses utilisation. The design of veterbei decoder is simulated using verilog HDL.Itsynthesized and implementation using Xilinx8.2 lise and spartanXC3S400Kit.*

Keywords: *Convolution encoder, constraint length, Code rate, Veterbi decoder, Veterbi algorithm, Verilog HDL, FPGA.*

I. INTRODUCTION

Convolution coding is coding schemes used in digital communication systems. It gives an alternative approach to block codes for transmission over a noisy channel. The process of adding the redundant bits or information is known as channel coding. There two types of coding namely block and convolution code. The block codes can be applied to a continuous data stream as well as to blocks of data.IS-95,a wireless digital cellular standards for CDMA., employs convolution coding. A convolution code works by adding some structured redundant information to user's data and then correcting error using this information.

Viterbi decoding algorithm was developed by Andrew J. Viterbi in 1967.It is used as a decoding technique for convolutional codes as well as the bit detection in storage devices in many places. The algorithm operates by forming trellis diagram, which is eventually traced back for decoding the received information. Some of the applications of Viterbi decoder include mobile communication, satellite communication, digital cellular telephone etc...

II. CONVOLUTION ENCODER AND VITERBI DECODER SYSTEM

System Architecture

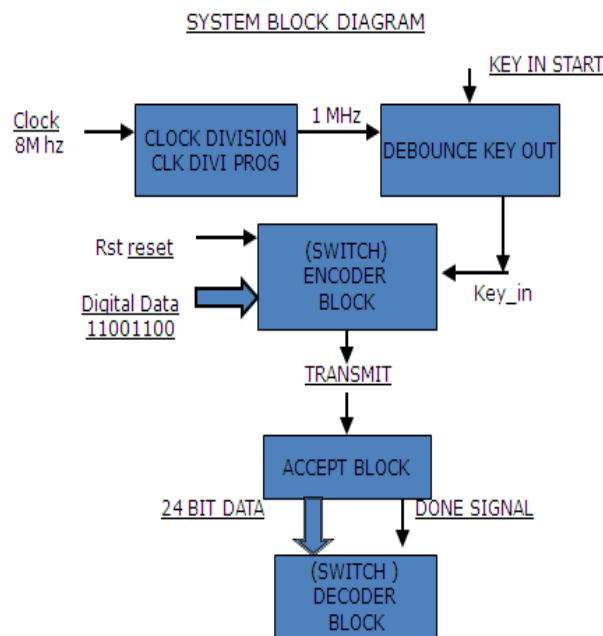


Fig 1: System Architecture

A. Encoder

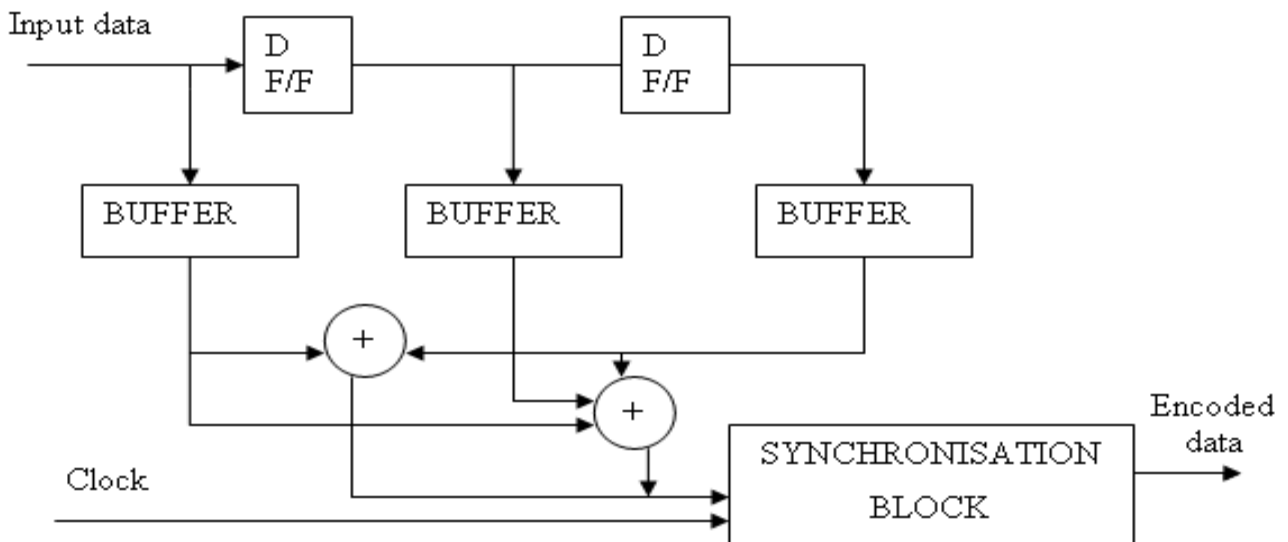


Fig.2 Convolution Encoder for K = 3

Description:

For above (2,1,2) encoder,

- $N=2$, for each input bit we get 2 encoded bits at the output.
- $K=2$, constraint length is 2.

The diagram of convolutional (2,1,2) encoder is shown in fig. no. 3.1. The encoder is a simple shift register consists of D flip-flops. The outputs of the each flip-flops are connected to EX-OR gates according to generator polynomial equation. The message bits are applied to the input of the shift register. The decoded bit stream is obtained at the output.

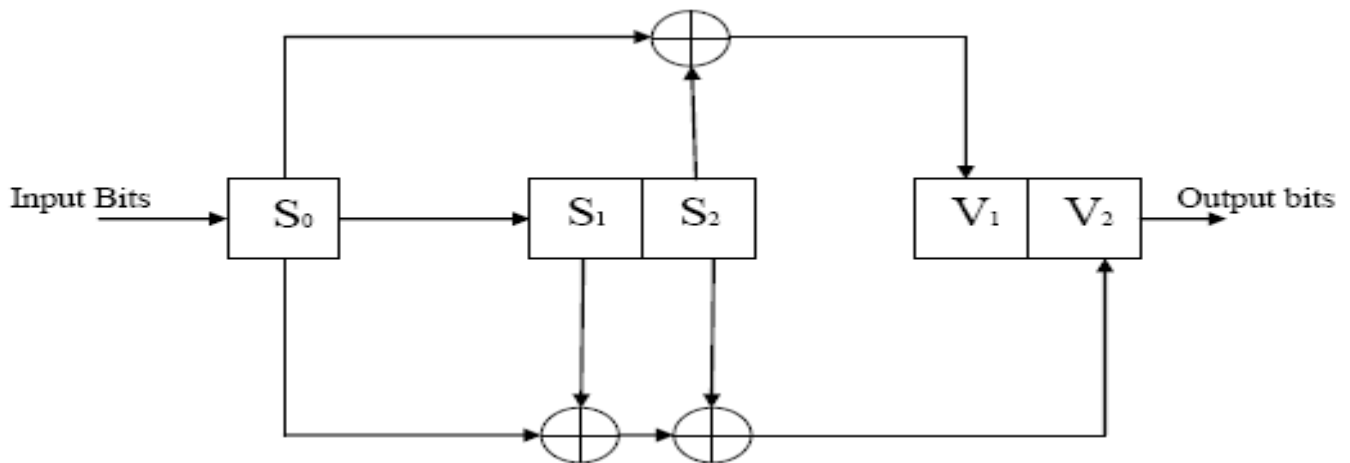
Convolution Encoder:

Fig.3 Convolution Encoder for K = 3

A convolutional coding is done by combining the fixed number of inputs bits. The input bits are stored in the fixed length shift register and they are combined with the help of mod-2 adders. This operation is equivalent to binary convolution and hence it is called convolution coding. The concept is illustrated with help of above example.

Whenever the message bit is shifted to position 'S', the new values of V1 and V2 are generated depending upon S0, S1, and S2. S1 and S2 store the previous two message bits. The current bit is present in S1. Thus, equation becomes,

$$V1 = S0 \text{ XOR } S1 \quad \text{and} \quad V2 = (S0 \text{ XOR } S1) \text{ XOR } S2$$

The output switch first samples V1 and then V2. The shift register then shifts contents of S1 to S2 and contents of S0 to S1. Next input bit is then taken and stored in S0. Again S1 and S1 are generated according to this new combination of S0, S1, and S2. The output switch then samples V1 and V2.

For every input message bit two encoded output bits V1 and V2 are transmitted. For a single message bit, the encoded code word is two bits for this convolution encoder.

Number messages bits $k=1$,

Number of encoded output bits for one message bit, $n=2$.

The following table shows the incoming bit S0 and status of encoder i.e. S1 and S2 corresponding output.

Input Bits	Current State of Encoder			Next State of Encoder			Output Bits	
	S0	S1	S2	S1	S2	V1	V2	
0	0	0	0	0	0	0	0	
1	0	0	0	1	0	1	1	
0	0	0	1	0	0	1	1	
1	0	0	1	1	0	0	0	
0	1	0	0	0	1	0	1	
1	1	0	0	1	1	1	0	
0	1	1	1	0	1	1	0	
1	1	1	1	1	1	0	1	

From table above, the state diagram is as shown below.

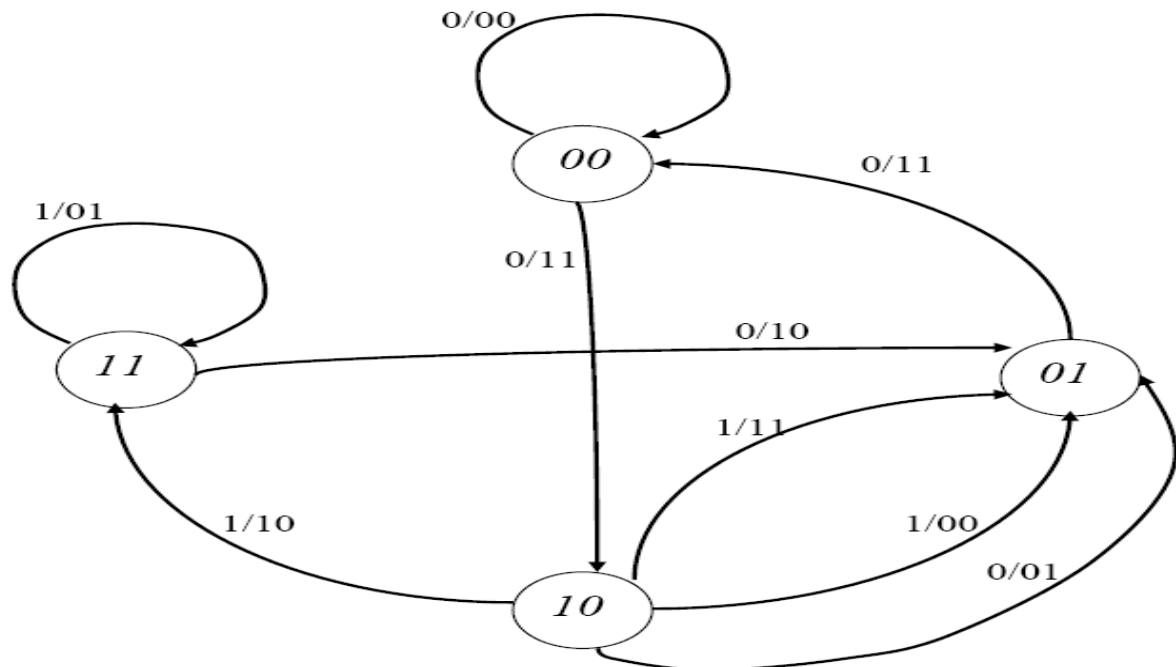


Fig.4 State Diagram of Convolutional For K = 3

III. VITERBI DECODER

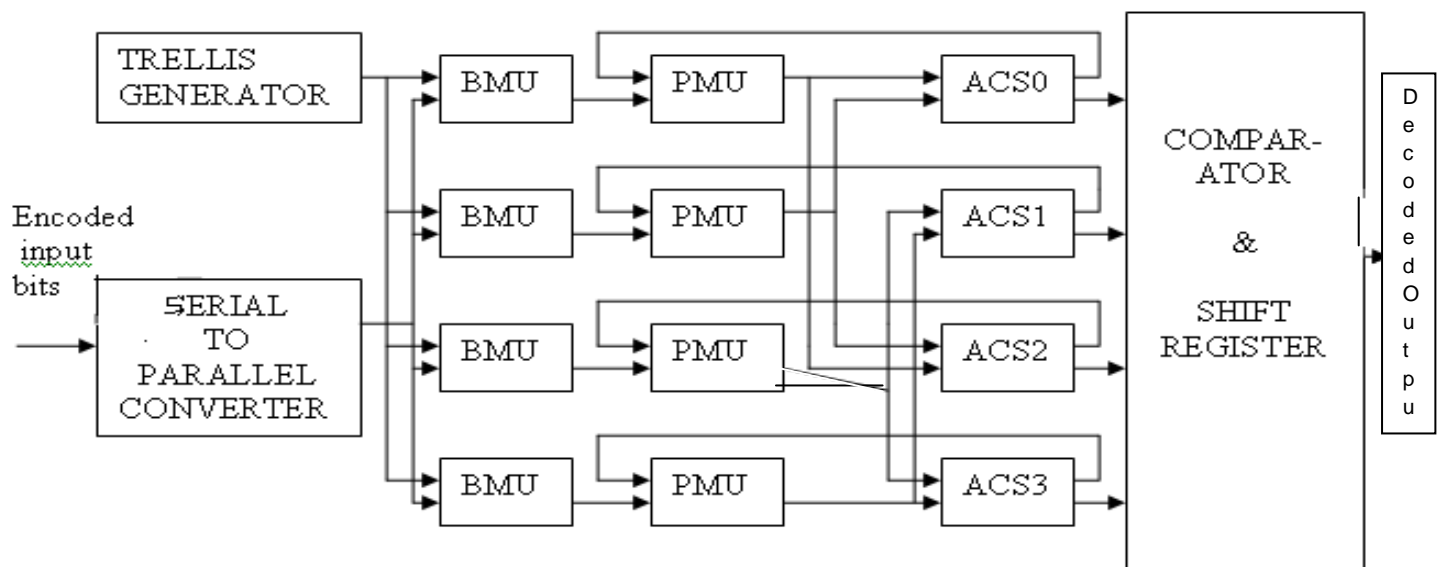


Fig.5 Block Diagram of Viterbi Decoder

The receiver receives the serial encoded data and converts it into 2-bit parallel data. This parallel data is now feed to the subsequent blocks. Trellis Generator generates the predefined sequence which is used to calculate the branch metric unit.

- 1. Serial to parallel converter:** The input bit to the decoder is serial in nature. The output of encoder is n bits for one input bit. As the input bits to the decoder are serial in nature, therefore to get required n bits we convert the serially obtained bits into n bit parallel form. For (2,1,2) Encoder The input bits are converted to 2 bit parallel form. The output of serial to parallel converter is to be compared with all the possible output of the code trellis.
- 2. Branch metric unit:** The main function of this unit is the calculation of the branch metric for each input to the decoder. As trellis diagram is fixed for the particular decoder, from this trellis logical equation are derived to calculate branch metric.

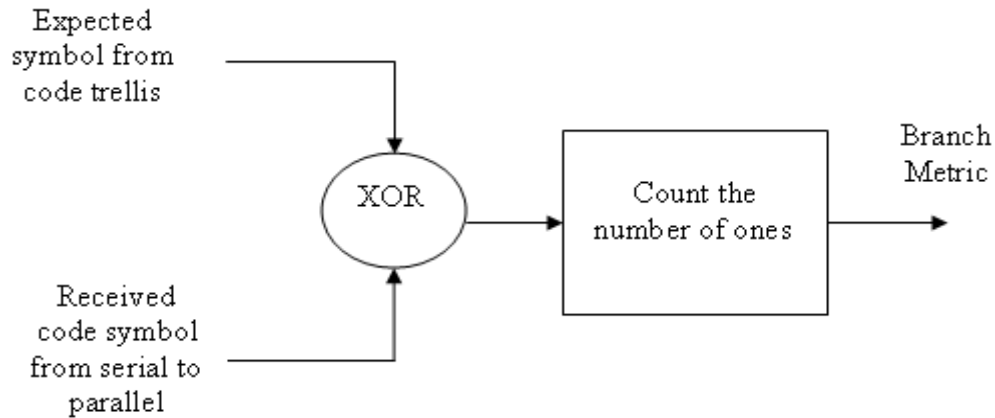


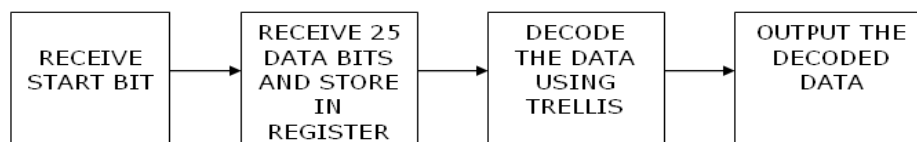
Fig . 6

3. **Path metric unit:** This unit has two inputs one from the Branch metric unit and second is the previous path metric from ACS unit. This unit just adds the two inputs and creates the new path metric.
4. **ACS (Add Compare & Store unit):** For this unit there are two input path metrics. ACS compares the two path metrics and gives out the minimum path metric at the output with its data bit. The data bits are stored.
5. **Comparator and shift register:** This unit accepts the path metric selected by every ACS unit for every cycle and gives out minimum path metric with its data bits.

Fig.7. Viterbi Decoding

Transmitter:

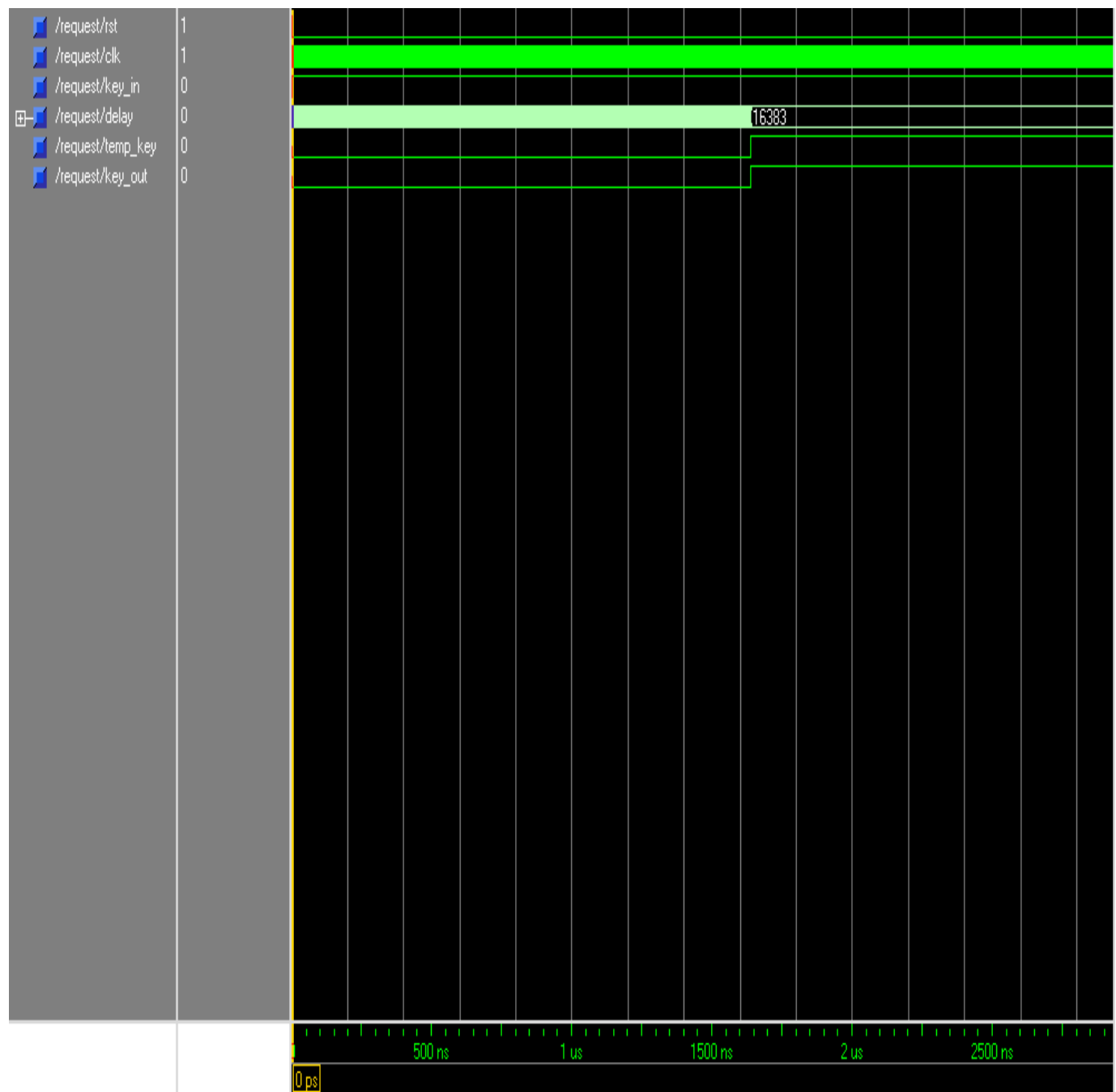
1. Generate 1MHz clock from the clock of the kit.
2. Give start signal for encoding after giving 16 msec delay for key de bounce.
3. Take the input data in the form of 8 bits.
4. Take the input data and do the Convolution encoding.
5. After encoding transmit the data serially in asynchronous mode of transmission. Start and stop bits are also added while transmission.

Receiver:

1. Wait for falling edge to be detected, after detecting falling edge sample after 52µsec if sampled bit is 0 then start bit is being detected.
2. Now sample the next 25 bits after every 104 µsec.
3. After 25 bits are received check that next bit received is STOP bit.
4. Give the received data to the Viterbi decoder for decoding.
5. After decoding output the data which is original information transmitted.

IV. RESULTS AND DISCUSSION

The Convolutional encoder and Viterbi decoder is simulated and implemented using Verilog HDL and Xilinx Spartan 3E Kit. The Viterbi decoder decodes the original input sequence by using Viterbi algorithm. The proposed design of viterbi decoder occupies fewer amounts of resources when compared with conventional design; it means that it has less hardware complexity. The simulation result, device utilization summary and FPGA Editor of two different encoder and decoder is shown in figures. The power analysis for viterbi decoder is done by Xilinx X power analyze. The power consumed by the viterbi decoder which is less compared to previous result. The device utilization summary shows that how much resources like LUT's, flip flops, input and output is utilized by the design of viterbi decoder for the convolutional encoder for K=3 is shown in figure. The FPGA Editor shows that the amount of area which is occupied by the design of viterbi decoder. The comparative analysis between two constraint lengths. In this table G1 and G2 represents generator polynomial of convolutional encoder. It denotes the sequence of connections (a one representing a connection and a zero no connection) from the memory elements (flip flops) of a shift register to an output. The comparative analysis result shows that an constraint length increases hardware complexity increases.

OUTPUT OF REQUEST KEY

OUTPUT OF ENCODER:

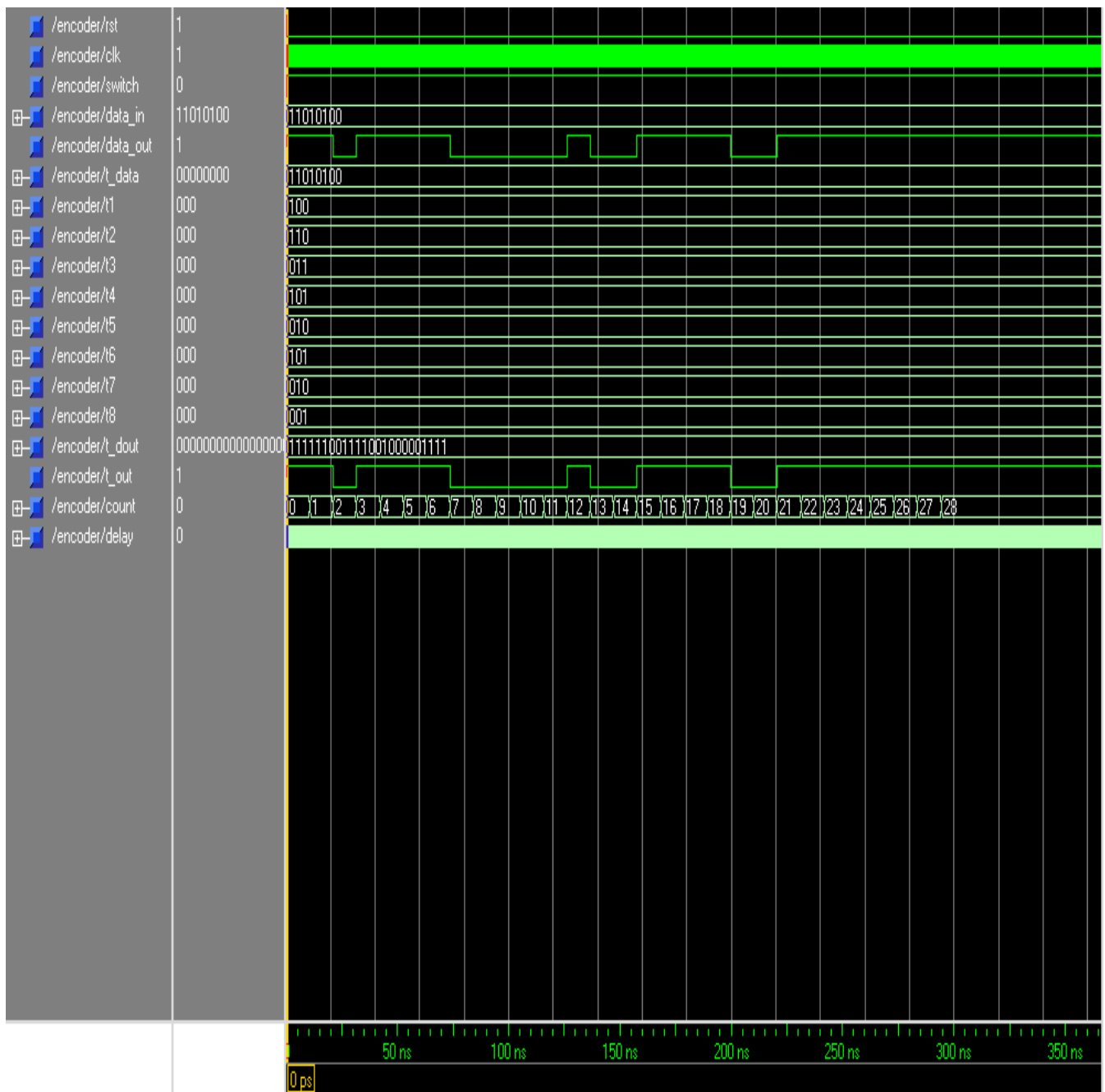
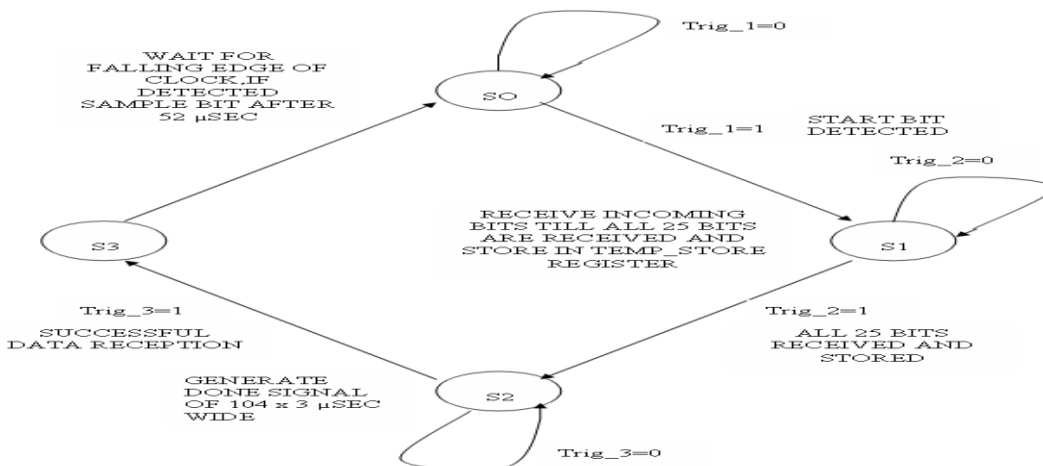


Figure: Simulation Result of Convolution Encoder K=3

STATE DIAGRAM FOR ACCEPT DATA AT RECEIVER



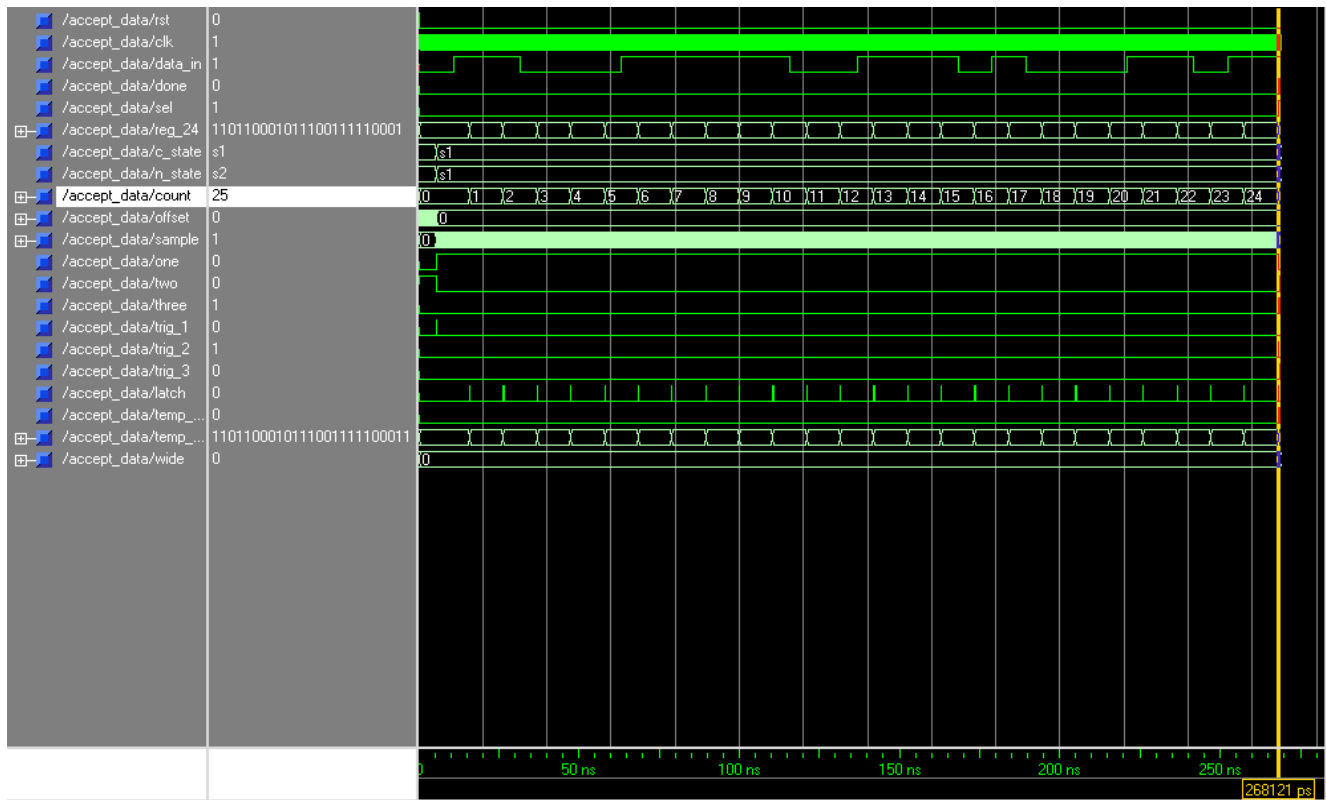


Figure: Simulation Result of Convolution Decoder K=3

V. CONCLUSION

1. The design of veterbi decoder for convolution encoder is synthesized and implementation on Spartan XC3S400 Kit.
2. Veterbi decoder can remove unwanted noise in the incoming data strem by decoding it.
3. Even though veterbi decoder is used in commercial wireless communication purpose.
4. The main complexity of veterbi decoding, confines its application to convolution codes with constraint length, not exceeding 7.
5. The future work is to improve the speed of decoding using VLSI technique, folding retiming.

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Sudhakar B. Chougule completed his Bachelor of Engineering in Electronics Engineering from Tatyasaheb Kore Institute & Technology in 1998 and presently pursuing M.E. from K.I.T. Kolhapur. He is having teaching experience of 14 years with specialization in Basic Electronics, RF circuit and design, Optical fiber communication and Microwave Engineering and Instrumentation.