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Analysis and Comparison of Adders in Real Time Conditions using Backend Process

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Abstract: ***The proposed paper is to design a high speed low power VLSI adder subsystem, for usage in ASIC's and low power and high speed applications. The speed performances in several ASICS rely on adder's performance. In this design, an error tolerant adder subsystem is proposed. The proposed project also involves the study of various adders, power delay comparison and study for design of full adders with optimum number of transistors to increase speed of the circuits. The design is approached through backend EDA tools (cadence/synopsis) under real time simulation conditions. The conventional 28T CMOS full adder will be replaced by 10T full adder and 14T full adder. By optimization of transistors, and comparison of PDP (Power Delay Product), which is the product of average power consumption and worst case delay, it is proposed for improvisation of speed along with low power consumption.***

Keywords: Adders, digital signal processing (DSP), error tolerance, high-speed integrated circuits, low-power design.

I. INTRODUCTION

The design of adder subsystem is the most focused area in VLSI design of processing units. So far there are a variety of such adders like RCA, CSA, and CLA. The design of high-speed and low-power VLSI architectures needs efficient arithmetic processing units, which is optimized for the performance parameters, namely, speed and power consumption. Adders are the key components in general purpose microprocessors and digital signal processors. They also find use in many other functions such as subtraction, multiplication and division. Furthermore, for the applications such as the RISC processor design, where single cycle execution of instructions is the key measure of performance of the circuits, use of an efficient adder circuit becomes necessary, to realize efficient system performance. Additionally, the area is an essential factor which is to be taken into account in the design of fast adders. Towards this end, high speed, low power and area efficient addition and multiplication has always been a fundamental requirement of high performance processors and systems. The major speed limitation of adders arises from the huge carry propagation delay encountered in the conventional adder circuits, such as ripple carry adder and carry save adder.

Arithmetic operations are widely used in most microelectronic systems. Addition is a fundamental arithmetic operation and is the base of many other commonly used arithmetic operations. Designing low-power VLSI systems has become an important performance goal because of the fast growing technology in mobile computation and communication. The world accepts analog computation, "Which generates good enough" results rather than totally accurate results. Also in digital VLSI systems, we do not get accurate results as in the case of communication systems the analog signals are sampled, digitized and transmitted over a noisy channel. Error may occur anywhere in this process. With the explosive growth the demand and popularity of portable electronics is driving designers to strive for smaller silicon area, higher speeds, longer battery life, and more reliability. Power is one of the premium resources a designer tries to save when designing a system. The aim to increases battery life of portable electronic devices is to decrease the energy expended per arithmetic operation, however lower power consumption does not necessarily bring about lower energy dissipation and higher performance. To perform arithmetic operations, a device can use up very low power by functioning at very low frequency but it may spend a very long time to finish the operation. Therefore, we

measure the energy dissipation and evaluate the performance of the system by calculating the Power-Delay Product (PDP), which is the product of average power consumption and worst case delay.

Also the performance of the processors in several application specific processors in terms of its speed is another important factor that relies totally on the adder's performance. Of course, not all digital systems can engage the error-tolerant concept. In digital systems such as control systems, the correctness of the output signal is extremely important, and this denies the use of the error tolerant circuit. However, for many digital signal processing (DSP) systems that process signals relating to human senses such as hearing, sight, smell, and touch, e.g., the image processing and speech processing systems, the error-tolerant circuits may be applicable. Taking the above considerations, an error tolerant adder design is proposed, which can be used in areas where a minimal amount of error is acceptable.

II. Calculation of Error Tolerant Adder

Overall Error (OE) OE = Oca – Oeta, where Oca is the result obtained by the adder, and Oeta denotes the correct result (all the results are represented as decimal numbers).

Accuracy (ACC) In the scenario of the error-tolerant design, the accuracy of an adder is used to indicate how "correct" the output of an adder is for a particular input. It is defined as A = (1-(E/Oca)) × 100. Its value ranges from 0% to 100%.

Minimum Acceptable Accuracy (MAA) Although some errors are allowed to exist at the output of an ETA, the accuracy of an acceptable output should be "high enough" (higher than a threshold value) to meet the requirement of the whole system. Minimum acceptable accuracy is just that threshold value. The result obtained whose accuracy is higher than the minimum acceptable accuracy is called acceptable result.

Acceptance Probability (AP) Acceptance probability is the probability that the accuracy of an adder is higher than the minimum acceptable accuracy. It can be expressed as AP = P (ACC > MAA), with its value ranging from 0 to 1.

III. Hardware Implimentation ETA

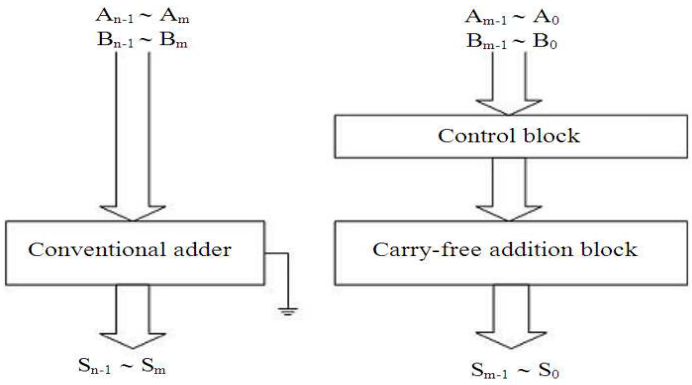

Fig.1 Logic Diagram of ETA Adder

The block diagram of the Error Tolerant adder that adapts to our proposed addition arithmetic is shown. This most straight forward structure consists of two parts: an accurate part and an inaccurate part. The accurate part is constructed using conventional adder. The carry-in of this accurate part adder is connected to ground. The inaccurate part constitutes two blocks: a carry-free addition block and a control block. The control block is used to generate the control signals to determine the working mode of the carry-free addition block. In addition, the Least Significant Bit (LSB) of the multiplier (bit B(O)) is used as control bit P for both accurate part and inaccurate part of the proposed adder.

For B(O) is one, the adder cells performs normal addition operation. For B(O) equals to zero, the adder Cells are brought into OFF state with NMOS and PMOS transistor driven by P brought into open state and the line from supply to ground is cut off,

thus minimizing leakage power dissipation. Based on the proposed methodology, an 8-bit Error tolerant adder is designed by considering 4 bits in accurate part and 4 bits in inaccurate part.

IV. PROPOSED WORK

In this paper, the study of various single bit and parallel bit adders is proposed. The functionality is verified and power and delay analysis using cadence tools is done. Apart from the different single bit and parallel adders, a new power saving parallel adder (ETA) is designed. The functionality and analyses are done. The design and analyses are done in analog environment of cadence tools. The different single bit adders for which the analyses are done are

1. 8 Bit RCA Parallel Adder
2. 8 Bit CLA Parallel Adder
3. 8 Bit CSA Parallel Adder
4. 8 Bit ETA Parallel Adder

V. PROCEDURE

1. The schematic part is entered manually using the gpdk180 technology library files.
2. Symbols can be created for each individual component and can be added to the library and can be used in larger designs.
3. The connections can be checked using the check option to find out any wiring that are missed out or not properly connected
4. The Functionality of the design is checked by performing the transient analysis
5. The outputs and inputs to be plotted are selected from the schematic.
6. The power and timing analyses are done using the tool Spectra by the procedure specified by the cadence flow

VI. RESULTS

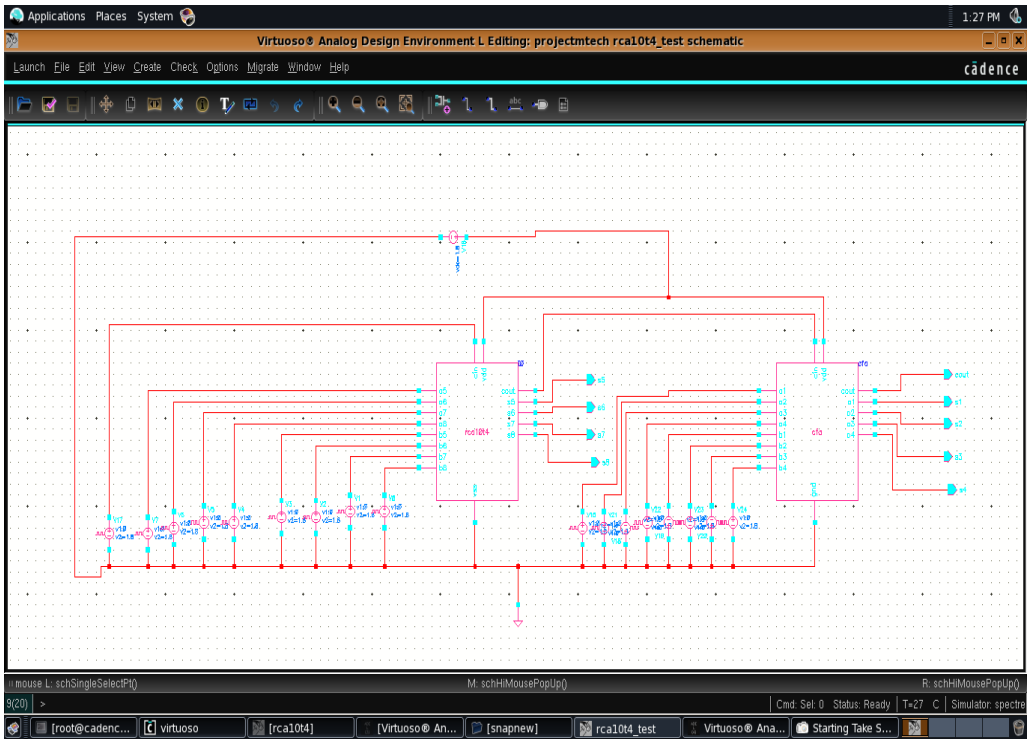

Fig.2 Block Diagram of ETA Adder

ETA Adder consists of a Carry Free Addition part i.e. CFA and a normal RCA Adder. The first 4 MSB bits are given to RCA Adder to preserve the correctness and the remaining LSB bits are given to the CFA Adder. In the RCA Adder, a 10 Transistor Full Adder is used.

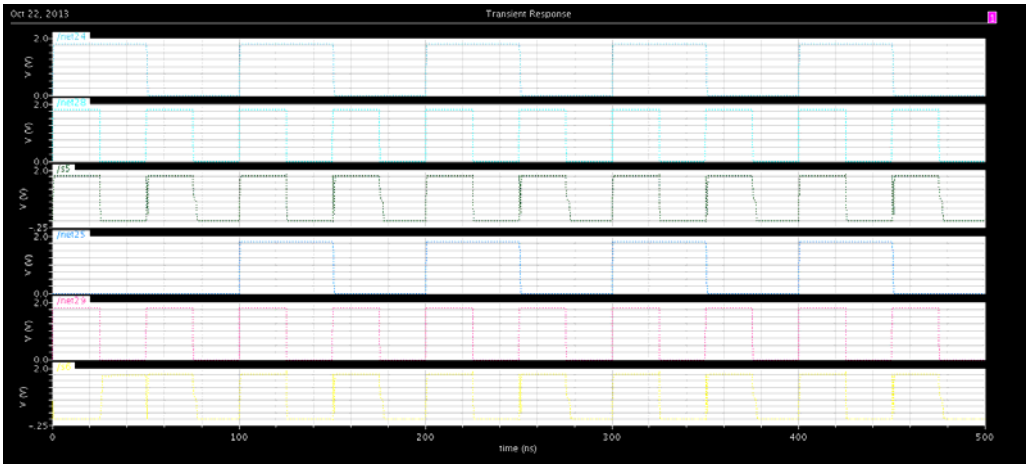

Fig.3 Output waveform of ETA Adder

The Output waveform of the 8 Bit ETA Adder is shown in figure 62, a5, b5, s5, a6, b6, s6 are shown in the graph from top to bottom rows..

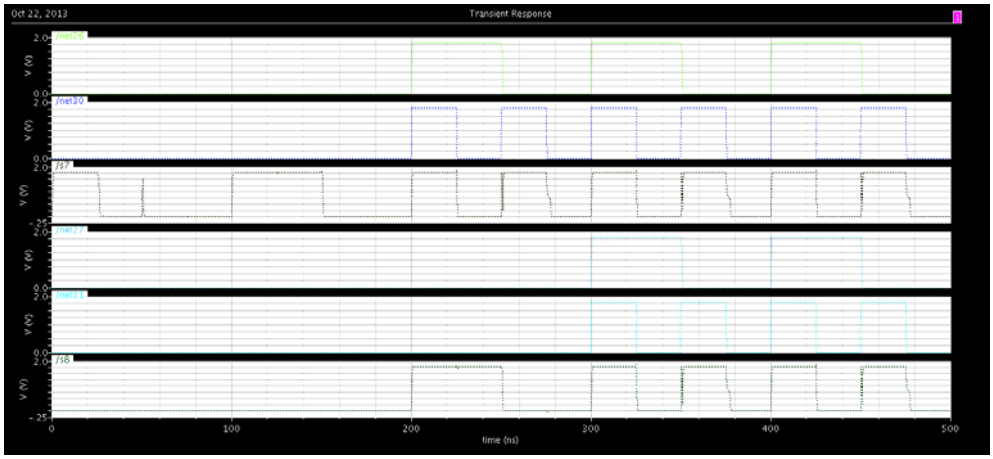

Fig. 63 Output waveform of ETA Adder

The Output waveform of the 8 Bit ETA Adder is shown in Fig 63, a7, b7, s7, a8, b8, s8 are shown in the graph from top to bottom rows.

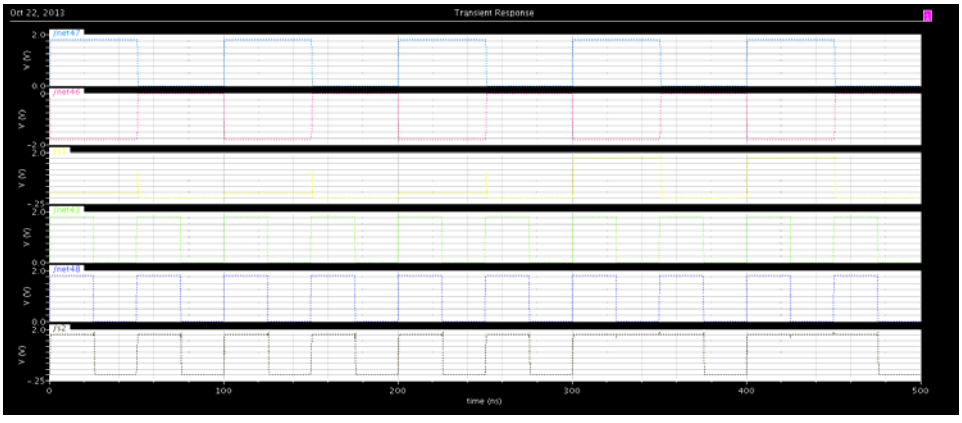

Fig. 64 Output waveform of ETA Adder

The Output waveform of the 8 Bit ETA Adder is shown in Fig 64, a1, b1, s1, a2, b2, s2 are shown in the graph from top to bottom rows.

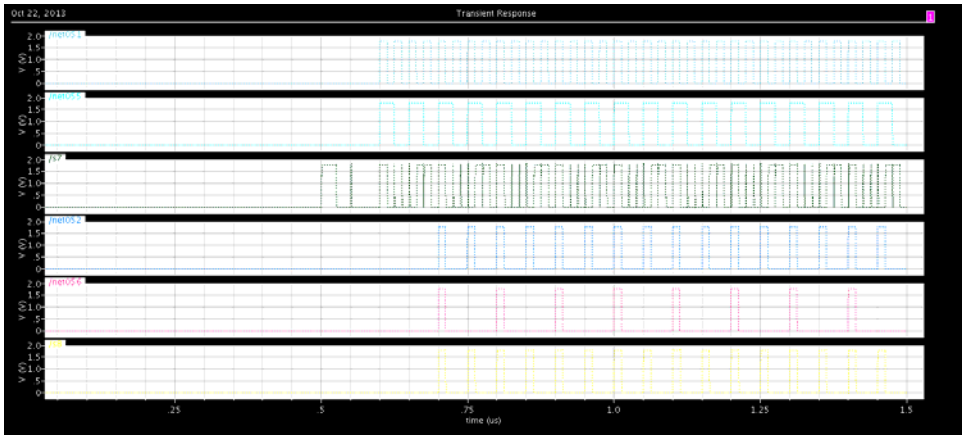

Fig. 65 Output waveform of ETA Adder

The Output waveform of the 8 Bit ETA Adder is shown in Fig 65, a3, b3, s3, a4, b4, s8 are shown in the graph from top to bottom rows.

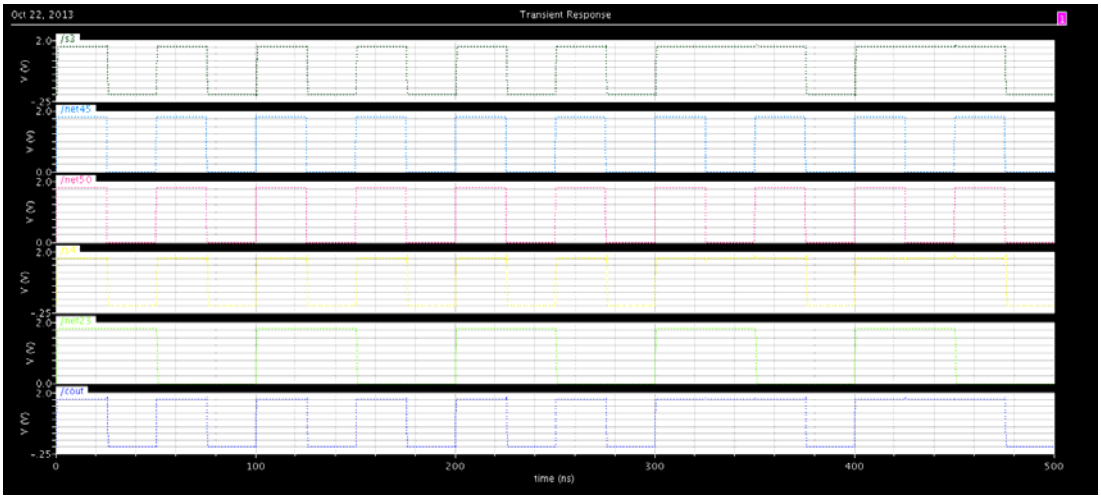

Fig. 66 Output waveform of ETA Adder

The carry in (c in – net 23) and carry out (c out) can be observed in Fig. 66.

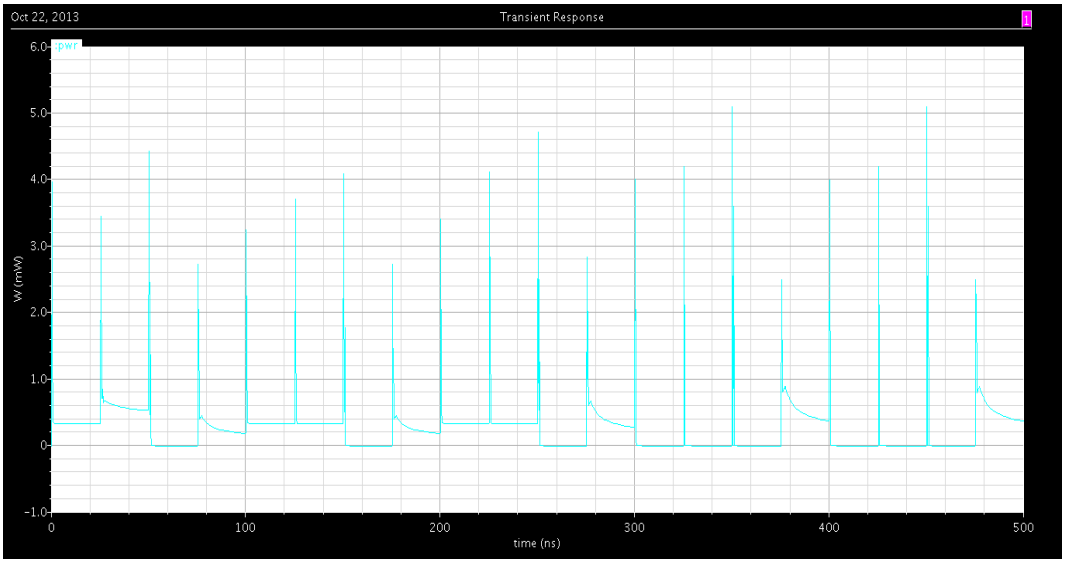

Fig. 67 Power waveform of ETA Adder

The Graph of the power consumed by the design after simulation is shown. Peak power consumption can be seen at the switching of the transistors. Peak value is 5.1mW.

VII. PDP Comparison of 8 Bit Parallel Adders

TYPE OF ADDER (8BIT)	Delay (ns)	Power Dissipation (µw)	PDP (e-12)	Transistor Count
RCA	637.9	166.0	105.742	224
CSA	328.5	721.9	237.144	428
CLA	300.8	700.9	210.830	556
ETA	25.5	250.2	6.3801	172

Table 1 PDP Comparison of 8 Bit Parallel Adders

VIII. Conclusion

From the results, the 10T Adder has better performance in terms of PDP (Power Delay Product) than the others. However for customized applications in which some need less delay and some with less power consumptions, the adders can be chosen accordingly. In the case of ETA Adder performance is far better than other adders when compared in terms of Power Delay Product. The Layout for the ETA is done and GDSII data is also extracted.

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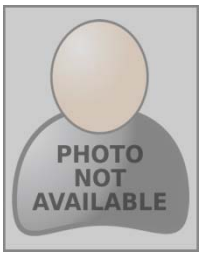
Author(s) Profile



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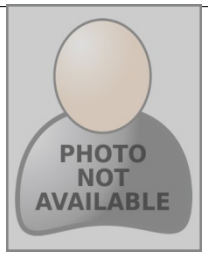

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