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Design and Implementation of Turbo Decoder and Rake Receiver

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Abstract: ***In the modern era of electronics and communication decoding and encoding of any data(s) using VLSI technology requires low power, less area and high speed constraints. The turbo decoder with necessary parameters for wireless communication is an attempt to reduce the power and at the same time increase the speed compared to normal decoder. A rake receiver, which resolves multipath signals corrupted by a fading channel, is the most complex and power consuming block of a modem chip. The Turbo decoder is typically one of the major blocks in a LTE wireless receiver. The combined performance of the turbo decoder along with the rake receiver is used to minimize the power consumption. The main objective of this project is to design and implement the UMTS receiver using FPGA hardware. This paper focuses on developing the rake receiver and the turbo decoder. The FPGA implementation of this paper is performed using Verilog. The simulation of the receiver is done by using Model Sim6.4a and Synthesis and implementation is done by using Xilinx 9.1i Spartan 3E kit. The performance of the coding is analysed from the result of timing simulation using Xilinx.***

Keywords: VLSI, UMTS, Rake receiver, turbo decoder.

I. INTRODUCTION

The fundamental requirement of most wireless communications providers world-wide is to deliver communication links that provide uncorrupted data, voice or video with minimum delay and power consumption. Turbo codes have been proposed for wireless communications, such as the universal mobile telecommunication system (UMTS) for the third generation of mobile communications. With the application of turbo coding to more communication systems, low complexity implementation of turbo decoder becomes a more popular and challenging topic. Therefore, implementing an efficient turbo decoder with low complexity, short delay, and insignificant performance degradation is currently a quite challenging task. A rake receiver, which resolves multipath signals corrupted by a fading channel, is the most complex and power consuming block of a modem chip. Therefore, it is essential to design a rake receiver be efficient in power. A rake receiver also includes a time tracker for fine tuning of the timing and a combiner to combine the outputs of the fingers. The goal of this paper is to investigate the RAKE receiver in combination with a forward error correction turbo decoder, with regard to the energy consumption. These investigations are on a functional level and are not implementation dependent.

II. SYSTEM MODEL

In this paper, we consider a RAKE receiver in combination with a turbo decoder that is used in a mobile UMTS terminal. We consider only the reception of downlink traffic (transmission from base station to the mobile) because energy efficiency is more important for the mobile than for the base station.

A. Rake Receiver

A RAKE receiver is used for wideband code division multiple access systems (WCDMA). In a WCDMA system all the users transmit in the same band simultaneously. Each transmitted bit is spread by the transmitter by means of a multiplication with a kasami code. The length of this code is called the spreading factor. A larger spreading factor gives a better resistance against interference. The receiver despreads the received signal by multiplication with exactly the same kasami sequence code. The results of all multiplications are added. This process of multiplication and addition is called correlation. A RAKE receiver [14] has multiple fingers to correlate the received signals from different paths with different delays, and combines the results of the different paths to construct one output signal. The block diagram of a RAKE receiver is shown in Figure 1.1.

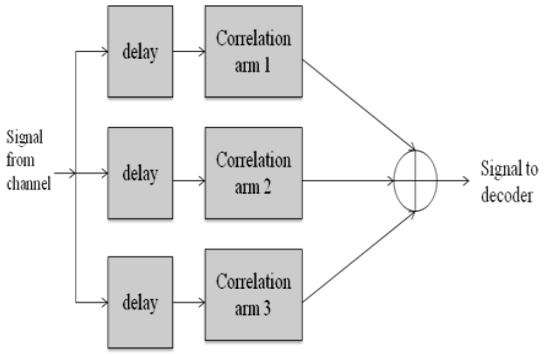

Fig. 1 Block diagram of Rake receiver

There are different types of code generation techniques. Mainly the following types of code sequence are used in Rake receiver design. These are

(a) Gold code sequence.

(b) Pseudo noise Sequence and

(c) Kasami sequence.

Here the kasami sequence and pseudo noise sequence have been described. There are two sets of Kasami sequence. These are small set and the large set. The large Set contains all the sequences in the small set. Only the small set is optimal in the sense of matching Welch's lower bound for correlation functions. Kasami sequences have period $N = 2^n - 1$, where n is a nonnegative, even integer. Let u be a binary sequence of length N, and let w be the sequence obtained by decimating u by $2^{n/2} + 1$.The small set of Kasami sequences is defined by the following formulas, in which T denotes the left shift operator, m is the shift parameter for w, and $\oplus$ denotes addition modulo 2. The small set contains $2^{n/2}$ sequences. A small set Kasami sequence is expressed as

$$k_{x(u,n,m)} = \begin{Bmatrix} u, & m = -1 \\ u \oplus T^m w, & m = 0, \ldots, 2^{\frac{n}{2}} - 2 \end{Bmatrix} \quad (1)$$

For mod (n, 4) = 2 the large set of Kasami sequences is defined as in equation 2. Let v be the sequence formed by decimating the sequence u by $2^{n/2+1}+1$. The large set is defined by the following equationn , in which k and m are the shift parameters for the sequences v and w, respectively. Large Set of Kasami Sequences for mod (n, 4) = 2 is expressed as

$$k_{L(u,n,m)} = \begin{Bmatrix} u, & k = -2; m = -1 \\ v & k = -1; m = -1 \\ u \oplus T^k v, & k = 0, \ldots, 2^n - 2; m = -1 \\ u \oplus T^m w, & k = -2;\ m = 0, \ldots, 2^{\frac{n}{2}} - 2 \\ v \oplus T^m w, & k = -2;\ m = 0, \ldots, 2^{\frac{n}{2}} - 2 \\ u \oplus T^k v \oplus T^m w, & k = 0, \ldots, 2^n - 2; m = 0, \ldots, 2^{\frac{n}{2}} - 2 \end{Bmatrix} \quad (2)$$

Where, *n* is the degree of the Generator polynomial, we can specify the Sequence index as an integer vector [*k*,*m*]. In this case, the output sequence is from the large set. The range for *k* is [-2,..., 2n - 2], and the range for *m* is [-1,…,2n/2 - 2].

The pseudo noise sequence generator consists of an linear feedback shift register. It generates the sequence of numbers that approximates the properties of random numbers. It generates the pseudo noise sequences.

B. Turbo Decoder

A turbo decoder is a forward error correcting decoder, which uses the soft values of a RAKE receiver as input and produces hard bits (0 or 1) on the output. The architecture of a turbo decoder [2] is shown in Fig. 2. The turbo decoder consists of two blocks. They are Add Compare Select Unit (ACSU) and Survivor Memory Unit (SMU). All these blocks are designed simulated and synthesized using Xilinx ISE.

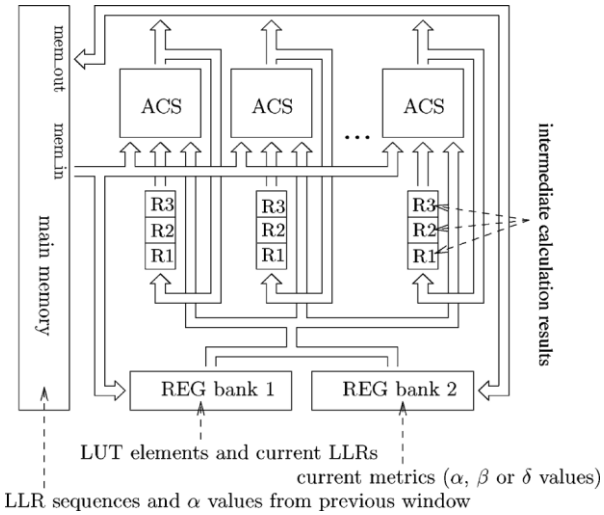

Fig.2 Turbo decoder architecture

1) *Add-Compare-Select Unit (ACSU):* The Add Compare Select Unit (ACSU) which adds the Branch Metrics (BM) to the corresponding Path Metrics (PM) compares the new PMs and then stores the selected PMs in the Path Metric Memory (PMM). At the same time, the ACSU stores the associated survivor path decisions in the Survivor Memory Unit (SMU).The PM of the survivor path of each state is updated and stored back into the PMM. The Block diagram of the Add Compare and Select unit is shown in the Fig.3

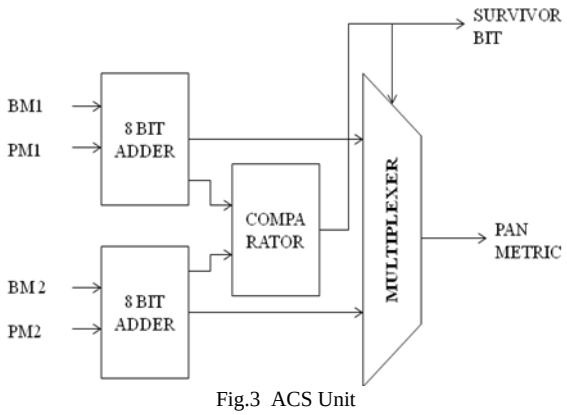

Fig.3 ACS Unit

State metric ($SM_{i,j}$) and Branch Metric ($BM_{i,j}$) are the two inputs to the Adder unit. Each butterfly wing is usually implemented by a module called ACS module. The two adders compute the partial path metric of each branch. The comparator compares the two partial metrics and the selector selects an appropriate branch. The new partial path metric updates the state metric of state p and the survivor path recording block records the survivor path. The adder unit which is proposed in the design consists of two 8 bit full adders. The output of the Branch metric unit (BMU) is added with the previous path metric and the obtained output is the new path metric for the next branch.

The output of the adder unit is given to the comparator. When the two inputs to the comparator are A=0011 0000 and B=1011 0000, then the output line A<B will go to high state i.e. less than state. If A and B are given as A=0111 1000 and B=0100 0000, then the output line A>B will go to the high state i.e. greater than state. Likewise all the input values are worked in the comparator. Here the A<B value is taken because it is the smallest value and hence the A<B state output is given to the next SMU unit.

The output of the comparator is given as the select signal for the multiplexer which is used to select the minimum path metric of the decoded message bit in the turbo decoder. The selector unit consist of four 2x1 MUX and the select signal for all the multiplexers are from the A<B output of the comparator. Hence the selector selects the minimum path metric value.

2) Survivor Memory Unit (SMU): The Survivor memory unit is designed by using the serial in- serial-out shift register and the length of the shift register depends on the length of the convolution encoder. The 4x4 memory unit is used to store the minimum surviving path and the clock signal of the SMU are the ACSU output for a constraint length of 3. The 8-bit output of the selector unit is the input of the SMU. The SMU was designed as 4x4 shift register using D flip-flop. Each bit is stored in each of the D flip-flop. Similarly all the 8 shift registers store one bit each. The input of D flip-flop and clock is the D flip-flop GND PULSE and CLK GND PULSE and the output for the q_1, q_2, q_3, q_4 ,q_5,q_6,q_7 and q_8 are shifting depending on the input value of D flip-flop and clock pulse. The number of memory stage depends on 2_{k-1} where k is the constraint length.

III. PROPOSED ARCHITECTURE

The proposed architecture for turbo decoder and the rake receiver is as shown in the Fig.4 and 5.It shows the number of gates, flipflops and multiplexers used in our design. The number of gates is considerably reduced by the efficient implementation of turbo decoder by VLSI technique.

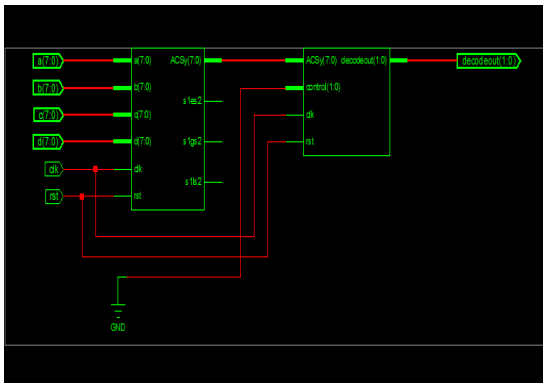

Fig.4 RTL view of Turbo decoder

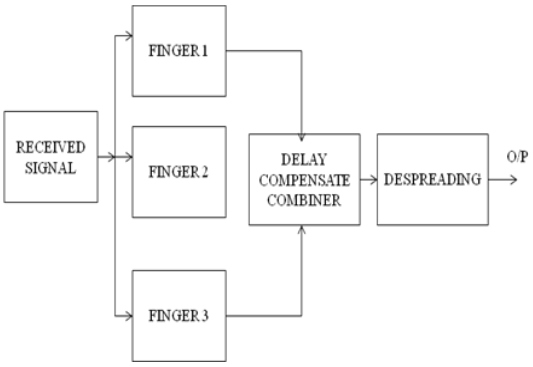

Fig.5 Proposed architecture for rake receiver

IV. RESULTS AND DISCUSSION

A. *SIMULATION RESULT*

The simulation result has been obtained by using Model sim software. The number of slices utilized by the turbo decoder on Spartran-3E are 13 out of 1920 which is considerably very economical and area saving. The number of bonded IOB's is 50 out of 66 available resources which is also very convenient. The design works at a frequency of 0.469GHz.

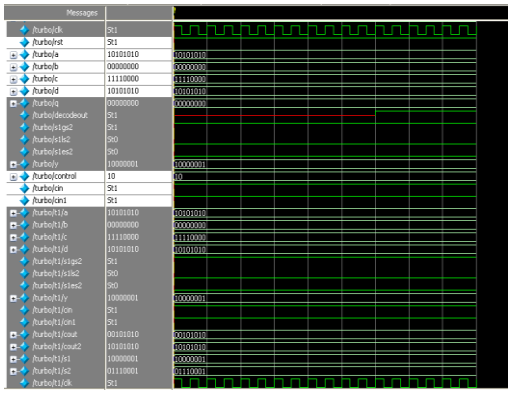

Fig.6 Simulation result of Turbo decoder

The number of slices utilized by the rake receiver on Spartran-3E are 125 out of 960 which is considerably very economical and area saving. The number of bonded IOB's is 11 out of 66 available resources which is also very convenient. The design works at a frequency of 0.408GHz.

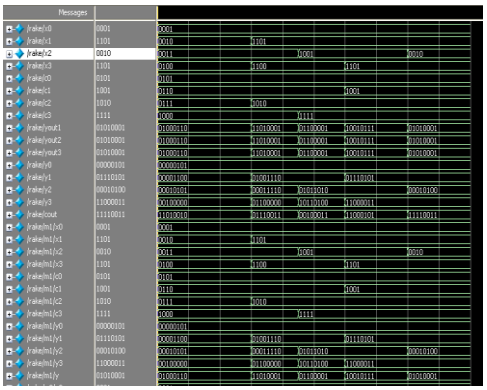

Fig.7 Simulation result of Rake Receiver using kasami sequence

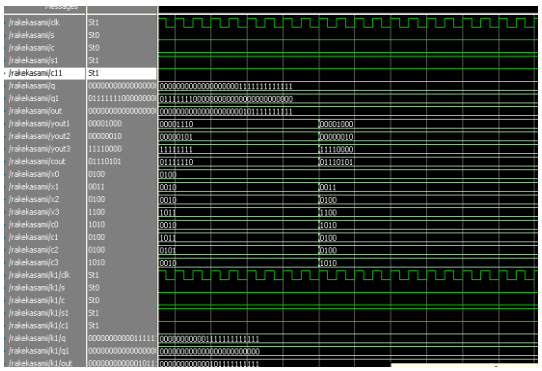

Fig.8 Simulation result of Rake Receiver using pseudo noise sequence

B. *SYNTHESIS RESULTS*

The receiver blocks are implemented on one of Xilinx's Spartran 3E FPGAs. Once the functional verification is done, the RTL model [11] is taken to the synthesis process using the Xilinx ISE 9.1i. In synthesis process, the RTL model will be converted to the gate level netlist mapped to a specific technology library [12]. This modified turbo decoder design is implemented on FPGA (Field Programmable Gate Array) family of Spartan3E. Here in this Spartan3E family many different

devices were available in the Xilinx ISE tool. In order to implement this turbo decoder and rake receiver , the device named as "XC3S500E" has been chosen and the package as "FT256" with the device speed as "– 4 ". The design of turbo decoder and rake receiver for low power [13] and high speed [14] is synthesized successfully and its results are analyzed.

After completion of synthesize, the entire circuit model is processed through Translate, Map, Place and Route successfully. Finally a UCF file of the target object is created which is prototyped with hardware FPGA Spartan3E hardware [15], through parallel connection using JTAG. Boundary Scan is performed followed by generation of PROM file.

The area results, timing results and power analysis results have been shown in Table I, Table II and Table III respectively. The results obtained by using Xilinx have been compared for both pseudo noise sequences and kasami sequences. The comparison result has been shown in Table IV.

TABLE I
Area Results

Area metrices for a XC3S500 E – FT256 device		
Parameter	**Used**	**%**
Number of Slices	28	1
Number of Slice Flip flops	14	0
Number of 4 input LUTs	50	1
Number of bonded IOBs	50	74
Number of GCLKs	2	4

TABLE III
Timing Results

Timing metrices for a XC3S500 E - FT256 device	
Parameter	Time (ns) Frequency (MHz) Memory(kb)
Minimum period	2.219
Maximum Frequency	469.704
Minimum input arrival time before clock	10.765
Maximum output required time after clock	12.359
Maximum combinational path delay	13.126
Total memory usage	152792

TABLE IIIII
Power Analysis Results

AVERAGE CONNECTION DELAY	:0.944ns
MAXIMUM PIN DELAY	:3.286ns
MAXIMUM DELAY	:0.074ns
GATE FANOUT	:22
NET DELAY	:3.176ns
PEAK MEMORY USAGE	:165 MB
DRIVE CURRENT	:204mA
VOLTAGE	:3.36V
POWER CONSUMPTION	:685.4mW

TABLE IVV
Comparison Table

	Using kasami sequences	Using PN sequences
Average connection delay	0.789ns	0.899ns
Maximum Pin delay	2.331ns	2.581ns
Fanout	38	37
Net skew	0.022ns	0.026ns
Power	250mW	375mW
Memory usage	88468kb	187580kb
Minimum period	2.450ns	2.362ns
Maximum frequency	408.115MHz	423.361MHz
Minimum input arrival time	4.466ns	4.517ns
Maximum output required time	15.905ns	18.606ns
Maximum delay	0.057ns	0.060ns

V. CONCLUSION

This paper presented a VLSI implementation of power optimization in turbo decoder and rake receiver. The proposed architecture is used to reduce the delay and power. The fast decoding can be achieved by turbo decoding approach. The combined performance of the turbo decoder along with the rake receiver is used to minimize the power consumption. The implementation of the turbo decoder and rake receiver is carried by Verilog HDL programming and synthesized in Spartan 3E using Xilinx ISE 9.1i. The device utilization of turbo decoder and the rake receiver is compared in terms of synthesis and implementation.

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