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IRAM: Study of an Upcoming Technology

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Abstract: ***The current architectures, applications and implementations of DRAM and SRAM necessitate the need of better performance memories. The implementation of Intelligent RAM (IRAM) provides a low cost memory by including a microprocessor in the fabrication process. IRAM uses the merits of both the semiconductor industries: memories and microprocessors to achieve optimum performance parameters. The paper evaluates the study of IRAM computations from point of view of DRAMs, its architecture, complexity, challenges and future scope.***

Keywords: DRAM, IRAM, microprocessor, SRAM, latency

I. INTRODUCTION

The growing disparity between DRAMs and microprocessors in the present world can be explained by the division of the semiconductor industry into microprocessor and memory fields [8]. The microprocessor field has improved with the rate of 60%/year and is known for increased speed. These offer fast transistors and various metal layers to facilitate efficient communication and uniform power distribution [4]. On the other hand, the memory field has shown a satisfactory improvement with the rate of 10%/year and is known for its increased capacity [8]. This field offers various polysilicon layers to reduce refresh rate by smaller memory cell size and low leakage currents [4]. This technological difference is Processor- Memory Performance Gap [7]. This gap which accounts for 50% creates a bottleneck problem in the overall system functioning [7]. Intelligent RAM is a concept which combines the above concepts to form a module containing advantages of both DRAMs and microprocessors for better performance. The word Intelligence stands for the microprocessor functioning and RAM stands for the memory [3].

II. LITERATURE SURVEY

DRAMs and SRAMs have been the conventional methods of memory designs and are being implemented worldwide on a large scale. But while dealing with the chip design, data transfer between the various components and its transfer rates become a factor of consideration. Improper data transfer can result in erroneous results. The first problem faced is matching the data transmission rate of the memory with the processor rate which is much faster than the memory [7]. The second problem is that since data bus is the main transfer medium, the memory has to travel through other devices to bring the data to processor for computation [7]. This results in idle cycles on the processor side which is a waste of resources. The factors contributing to the performance gap are latency and bandwidth [8]. Latency is the amount of time required for movement of data to and from the memory [10]. Bandwidth is the product of rate at which data is transferred or accessed and the width of the data bus [10]. An ideal processor-memory system has zero latency and infinite bandwidth [8]. Bandwidth incapability indirectly leads to increase in latency [8]. This lead to various researches in this field so that the processor and memories could be well matched and brought on the same designing platform. The Berkeley IRAM Project carried out in 1996-2004 has explored the ability of memory and processor being designed and fabricated on the same Integrated Chip [3].

III. DRAMs IN IRAMs

The possible approaches for IRAM implementation are:

1. Provide more cache memory to processors.
2. Put processor on SRAM.
3. Put processor in DRAM.

The approach selected is putting processor in DRAM since DRAM is much denser than SRAM which allows larger on-chip memory in IRAM implementation [3]. RAMs less expensive than Static RAMs which are made up of cells and do not retain their state indefinitely are known as Dynamic RAMs. DRAMs became commercially available despite their low yield in 1970 through Intel [9]. With the improvement in performance, availability in packages and cost effectiveness, these were available in 1973 [9]. Since then, they have shown an improvement with 10%/year which is not very acceptable [8]. Also, the required memory and operating system memory usage is improving at only half to three-quarters the rate of DRAM potential capacity [4]. In an attempt to overcome the bandwidth limitations, several advancements are made in DRAMS such as synchronous DRAM (SDRAM), enhanced SDRAM (ESDRAM), double data rate DRAM (DDR) and Rambus DRAM (RDRAM) [8]. The ultimate goal of IRAM technology is to reduce the latency but increase the bandwidth of DRAM configuration at the same time.

IV. MERITS

The advantages of this technology are evaluated in comparison to the conventional technologies available in the current market:

a) BANDWIDTH

In IRAM architecture, the processor and the memory are placed in the same chip. Thus the bus length is reduced leading to less opposition to data transfer from memory to the processor and indeed a high data transfer rate [3][6]. A DRAM has an internal bandwidth but this is used to full extent by this architecture. Each block has less number of I/O lines which reduce the internal bandwidth by a specific factor but still cater the external needs of the chip [6].

b) LATENCY

Ideal latency is difficult to achieve since every design has its limitations. However, the IRAM technology has the potential to lower the chip latency by a considerable amount since its architecture overcomes the drawbacks of the DRAM architecture. This can be further reduced by good floor planning, using faster topologies, and paying proper attention to the bus schemes used in the architecture [6].

c) ENERGY EFFICIENCY

IRAM has low power consumption with a higher performance which makes this technology more energy efficient than other conventional approaches. Also, since the whole circuit is on-chip, there is no need to drive external buses which consume high energy.

d) BOARD AREA AND COST

The processor and the memory are fabricated on a single chip which reduces the board area as well as the production cost. Though this increases the overall chip density, it can be used in portable devices and related applications.

e) MEMORY

IRAM offers a considerable flexibility in designing the chip as per the specifications of the application [1][6]. The size and width of on-chip DRAMs used can be varied [6].

V. DEMERITS

Though the IRAM technology has advantages, the disadvantages are as follows:

a) *ACCEPTANCE*

IRAM is a new architecture which is still in a novel state. DRAM is an economical model and so widely manufactured but IRAM on the other side is a customized model [1]. Despite its merits, the technology will take time to get a hold on the market.

b) TESTING

High complexity leads to higher level of computational testing. IRAM will need logic as well as memory testers which increases the testing time [1].

c) UPGRADABILITY

IRAM is designed on the DRAM platform. Thus, new memory with a better performance cannot be embedded into this design easily in future. This reduces the upgradability of this design.

d) HEAT DISSIPATION

As the technology scaling takes place with more devices on-chip thus reducing size of the circuit, heat dissipation becomes a major concern. In IRAMs, the DRAMs are embedded on chip along with vector processing blocks, which leads to overheating of the circuit at large data rates [3].

e) REFRESH RATE

Refresh rate is the time required by the IRAM to upgrade the data received. This is dependent on the operating temperature of DRAM such that refresh rates almost double with every 10 degree Celsius rise in temperature [1].

VI. CONCLUSION

The Intelligent RAM systems thus provide facilities which no other technology is providing with equivalent efficiency. Being a novel concept, more research and models can be expected in this field for an industrially acceptable architecture. IRAM is a globally computational system which will potentially require several software platforms for optimum performance considering parameters like latency, bandwidth, efficiency, cost, power requirements etc. which are described above. The focus of this system is to bridge the gap developed between the memories and processors successfully. However, the manufacturers will have to consider the statistics of cost along with the performance characteristics. If accepted globally, IRAM has the potential to become revolutionary implementation in the semiconductor industry.

ACKNOWLEDGEMENT

The paper represents an overview of the IRAM technology but not its implementation and testing. The topic needs to be further evaluated for the physical implementation of IRAM technologies in present day systems and the performance should be tested in comparison to other technologies available in the market.

References

1. David Patterson, Krste Asanovic, Aaron Brown, Richard Fromm, Golbus, Benjamin Gribstad, Kimberly Keeton, Christoforos Kozyrakis, Jason,"Intelligent RAM (IRAM): the Industrial Setting, Applications, and Architectures", Computer Science Division, University of California, Berkeley.
2. João Paulo Portela Araújo, "Intelligent RAM: a Radical Solution?" Departamento de Informática, Universidade do Minho
3. www.slideshare.com
4. David Patterson, Thomas Anderson, Neal Cardwell, Richard Fromm, Kimberly Keeton, Christoforos Kozyrakis, Randi Thomas, and Katherine Yelick, "A Case for Intelligent RAM: IRAM", Computer Science Division/EECS Department, University of California, Berkeley
5. Richard Fromm, David Patterson, Krste Asanovic, Aaron Brown, Jason Golbus, Ben Gribstad, Kimberly Keeton, Christoforos Kozyrakis, David Martin, Stylianos Perissakis, Randi Thomas, Noah Treuhaft, Katherine Yelick, Tom Anderson, John Wawrzynek, "Intelligent RAM (IRAM)" EECS, University of California,Berkeley
6. www.seminarsonly.com
7. www,prizedwriting.ucdavis.edu

8. Carlos Carvalho, "The Gap between Processor and Memory Speeds", Departamento de Informática, Universidade do Minho
9. www.wikipedia.org
10. www.technicalsymposium.com

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