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An Effective Test Data Delivery and Collection Method in NoC on Unicast Based Multicast Method

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Abstract: ***Network on Chip [NoC] is a new technology that embeds heterogeneous interconnected cores. It advantage over System on Chip [SoC] are that Network on Chip provides modularity, higher performance, better structure and compatibility with core design and reuse. Previous on chip interconnection network commonly assumed that each router in the network needs to contain buffers, where packets are transmitted from buffer to buffer within the network. This increases the complexity of the network design. To overcome this complexity, bufferless routing is used in unicast based multicast routing algorithm. This work discusses the impact of power reduction.***

Keywords: Network on Chip, System on Chip, Buffer Routing, Bufferless routing,Unicast Based Multicast.

I. INTRODUCTION

VLSI stands for Very Large Scale Integration. This field involves more and more logic devices into smaller and smaller area. VLSI categorized System on Chip, can integrate hundreds of cores into single chip this communicate by buses. A new paradigm is introduced; Network on Chip to solve the SoC problems. Network on Chip (NoC) is becoming a solution to nowadays bus-based communication infrastructure limitations. NoC architecture is possible to develop the hardware of resources independently as standalone blocks and create the NoC by connecting the block as element in the network. Moreover, the scalable and configurable network is a flexible platform that can be adapted to the needs of different workloads, while maintaining the generality of application development method and practices.

A two dimensional mesh interconnection topology is simplest from a layout perspective and the local interconnection between resources and switches are independent of the size network. Moreover, routing in a two-dimensional mesh is easy resulting in potentially small switches, high bandwidth, short cycle and overall scalability. A NoC consists of resources and switches that are directly connected such that resources are able to communicate with each other by sending messages. A resource is a computation or storage unit. Switches route buffer messages between resources. Each switch is connected to four neighboring switches through input and output channels. A channel consists of two one dimensional channel point to point buses between two switches or a resource and a switch. Switches may have internal queues to handle congestion. We expect the size of a resource to shrink with every new technology generation. Consequently the number of resources will grow, the switch-to-switch and the switch-to-resource bandwidth will grow, but the network wide communication protocols will be unaffected.

Arbitrary computation elements can be connected to the communication network. NoC based system may contain processor cores, DSP cores, memory banks, specialized input/output blocks such as Ethernet or Bluetooth protocol stack implementation, graphic processor, FPGA blocks etc. The size of the resource can range from a bare processor core to local cluster of several processors and memory connected via local bus.

The reuse of processor cores has been developed by defining bus interfaces. By defining network interfaces, NoC takes this concept further because it allows integrating an arbitrary number of resources into network. In bus based system adding a new has a profound impact on the performance of the rest of the system because the same communication resources are shared among more resources. In a NoC adding a new resource also means to add new communication capacity by adding new switches and interconnect.

A NoC provides support for message-passing in such cores, and also allows for spatial reuse, whereby communication among various modules can occur concurrently over a distributed collection of wires. There are several routing algorithm for communication to deliver the data. In routing algorithm unicast method is used to deliver the packet from single source to single destination, multicast method is used to deliver the single source to group of destination and broadcast method is used to deliver the single source to the entire destination.

The main contributions of the paper include: The test data delivery and the test responses are delivered along the reverse paths in the unicast based multicast tree back to the ATE, where test responses are compacted further on the way to the ATE without any extra hardware in the NoC is proposed.

II. Related Work

Many of the literature on NoC have discussed about various multicast techniques, buffered and bufferless routing techniques. A summary of these methods are discussed below;

In recent years,A number of routing algorithm are discussed for data delivery. AmiraliHabibi and Mohammad Arjomand [1] proposed multicast scheme. In a multicast scheme, a set of unique multicast tuples is in the form of m=<s, D> where s refers to an IP core sending a message to all cores in set. This approach includes two phases. In the first phase, the outgoing bandwidth of each source node is modified with respect to its multicast operations. Then, a heuristic algorithm to effectively map IP cores onNoC nodes based on the estimated outgoing bandwidth takes place.

Wenmin Hu and Zhonghai [2] proposed in tree based multicast. In a tree based multicast scheme is a tree structure built representing shortest path among nodes, and aloop-free distribution structure. There are two power efficient tree based multicast routing algorithms, Optimized tree (OPT) and Left XY-Right-Optimized tree (LXYROPT) are also proposed. XY tree-based (XYT) algorithm and multiple unicast copies (MUC) are also implemented on the router as base. Tree based multicast requests extra virtual channels. Tree based is inefficient.

Tzung-Shi Chen and Chih-yungchang [3] proposed in path based multicast scheme. In a path based multicast tree there are two proximity grouping they are graph based proximity grouping and pattern based grouping. Graph-based proximity is used to group the destination with locality together to construct several disjoint sub meshes. They are source to leader and leader to destination. Pattern-based grouping proposed to exploit the spatial locality of the destination set. Pattern based grouping is next presented to explore the destination set in order to form groups with proximity relations based on the pattern classification scheme. The path based multicast scheme is inefficient.

Po-Tsang Huang and Wei Hwang [4] proposed buffered routing. In buffered routing buffers are used to store and forward according to frequency of the receiver and the transmitter. Traditionally, In NoC Transmitter core and Receiver core must be synchronized, for this purpose buffers are used. Buffers store and forward the data according to the frequency of the receiver. In buffer communication there are different switching techniques. The buffer process leads to limitations in the existing system like increased memory size, increased power consumption and complexity in network design.

Thomas Moscibroda and OnurMutlu [5] proposed bufferless routing. In bufferless routing there are two techniques. They are flit-bufferless technique and wormhole bufferless technique. In flit-bufferless technique large packets are broken into small pieces called flits. The first flit, called the header flit holds information about this packet's route and sets up the routing behavior

for all subsequent flits associated with the packet. The head flit is followed by zero or more body flits associated with the packet. The head flit is followed by zero or more body flits, containing the actual pay load of data. The final flit, called the tail flit, performs some book keeping closing the connection between the nodes. And in Wormhole-bufferless technique, it does not dictate the route to the destination but decides when the packet moves forward from the router. Advantage of this bufferless routing an entire packet need not to be buffered to move on to the next node, increasing throughput and channel allocation are decoupled.

III. Problem and Formulations

The main problem addressed in this paper is formulated as follows: Most of the work on chip uses buffer for communication. A buffer stores the data and forwards the packet to the next node. Buffers on chip consume significant energy, occupies chip area and increases design complexity. The problem is to device a bufferless routing in order to reduce the complexity by using a bufferless unicast based multicast method.

IV. Proposed Method

To reduce the power in NoC based on bufferless routing in unicast based multicast scheme. In bufferless routing the buffer are eliminated and information regarding the frequency allocation is informed to the receiver core by the transmitter core by using the unicast based multicast scheme. A unicast based multicast scheme completes multicast by using multiple unicast. It delivers a packet from a single transmitter core to several receiver cores. Figure 1 and Figure 2 shows model of buffered and bufferlessrouting where T_1, T2, T3 …Tn and R_1, R2, R3…….Rnrepresent transmitting cores and receiving cores respectively.

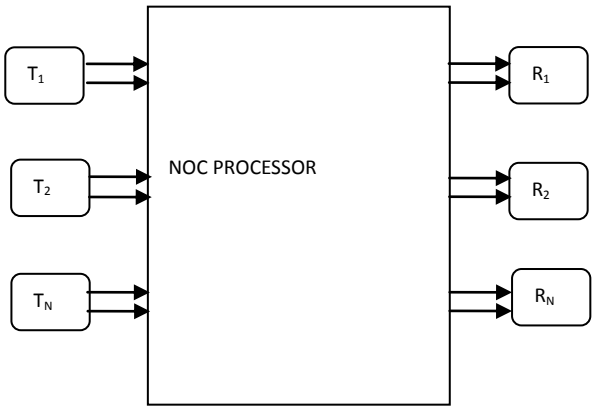

Figure 1Bufferless Routing

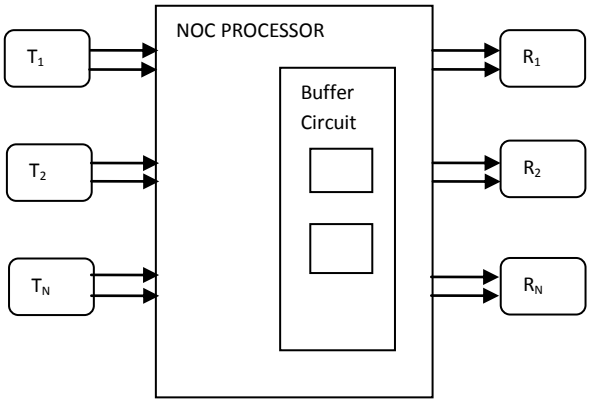

Figure 2 Buffered Routing

A. Automated Test Equipment Tool

Automatic or Automated Test Equipment (ATE) is any apparatus that performs tests on a device, known as the Device Under Test(DUT), using automation to quickly perform measurements and evaluate the test results. An ATE can be a simple computer controlled digital millimeter, or a complicated system containing dozens of complex test instruments (real or simulated electronic test equipment) capable of automatically testing and diagnosing faults in sophisticated electronic packaged parts or on Wafer testing, including System on chip and Integrated circuits.

B. Unicast based Multicast Method

A unicast-based multicast scheme completes multicast by using multiple unicast steps, therefore, it is not necessary to modify the unicast router architecture. Figure shows

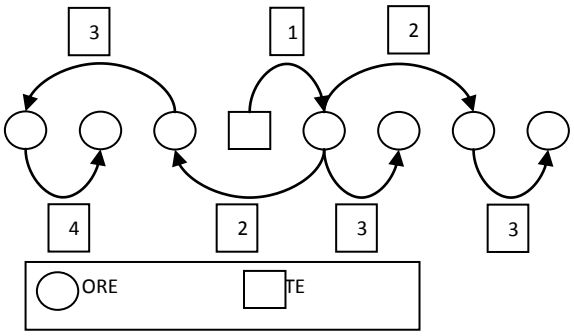

Figure 3 Unicast Based Multicast

C. Test Data Delivery Algorithm

A test packet is deliver to v_i ($1 \leq i \leq 8$) where all destinations and the source connected to the ATE are arranged as a dimension ordered chain.The dimension drder chain is divided into two equal parts D1 and D2. Cores deliver the test packet to D1 and D2 in bufferless routing, for that the frequency must be synchronized and deliver the packet based on the algorithm. Figure 4 and 5 shows the data deliver

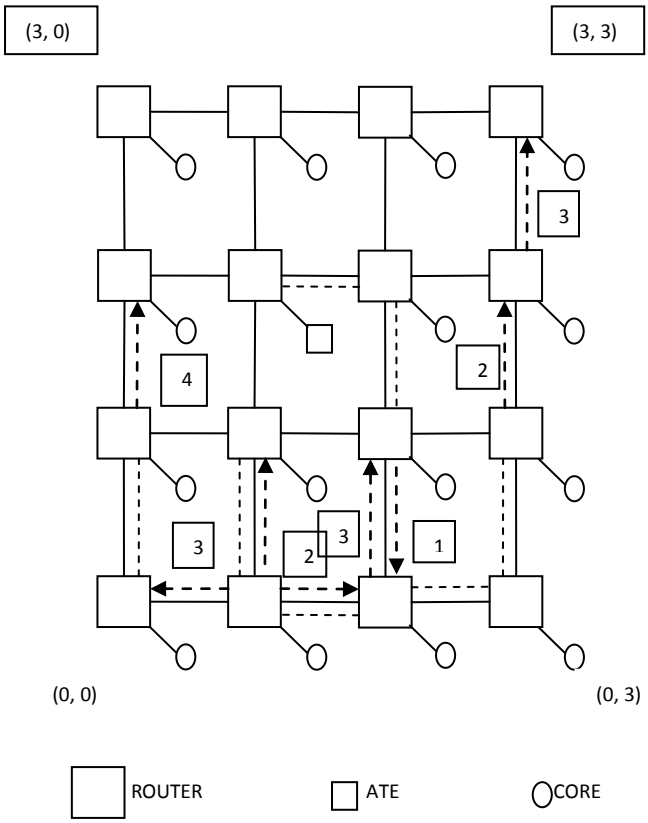

Figure 4Test Data Deliver in NoC

Figure 4 and 5 shows the cores are arranged in dimension order chain and data are delivered by using unicast based multicast scheme.

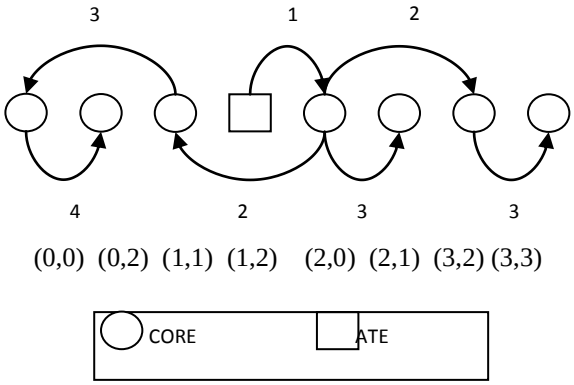

Figure 5 Test Data Deliver

Input:

Several numbers of cores

Output:

Data deliver to several numbers of cores

STEPS

1. The test vectors are arranged in dimension order (D).
2. The core (c) sequence divided into equal parts D1 and D2
3. Let c be the lower half of D1
   a.) While deliver the test packet for bufferless routing, synchronize the frequency and send to first node to D1.
   b.) Otherwise deliver the test packet for bufferless routing, synchronize the frequency and send to second node in D2.
4. Let c be the upper half of D2
   a.) While deliver the test packet for bufferless routing, synchronize the frequency and send to last node in D1.
   b.) Otherwise deliver the test packet for bufferless routing, synchronize the frequency and send to before last node in D2.

D. Test Response Collection Algorithm

The Test response collection graph use Y-X routing. The successors of a node become its predecessors, where the unique predecessor of an each node in the multicast tree becomes its unique successor. Test response of each test vector in a core is sent back to the node connected to the ATE as a single response packet. Figure 6 and 7 shows the response collection method of delivered data.

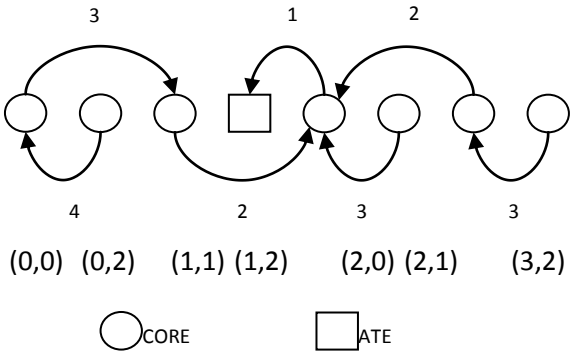

Figure 6 Test Response Collection

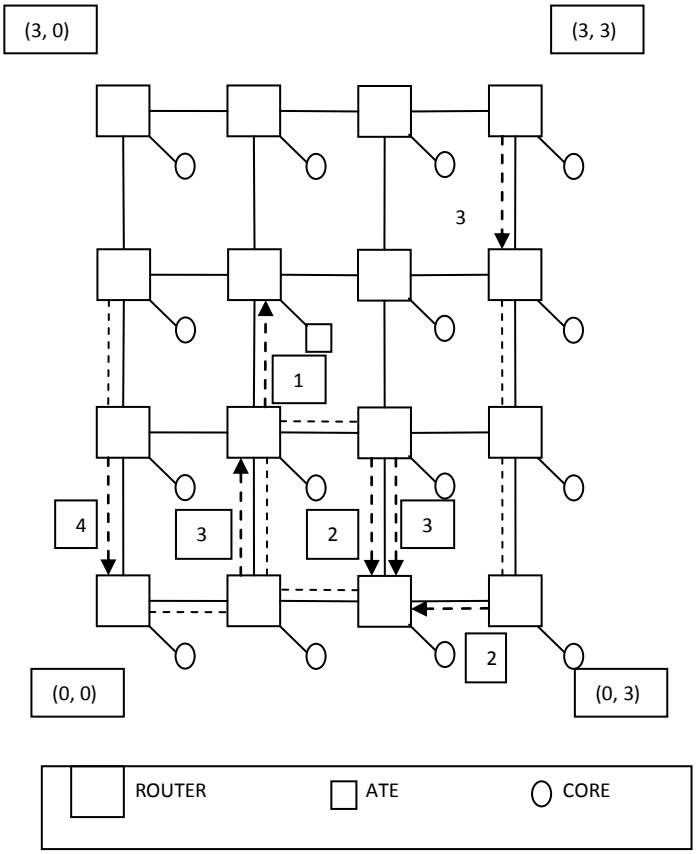

Figure 7 Test Response collection in NoC

V. CONCLUSION

A new NoC core testing scheme was proposed using a new unicast based multicast scheme and bufferless routing. Test generation for all cores in the on-chip network can be completed by merging all cores into a single circuit, according to which test stimulus data volume can be reduced significantly that was formulated into a unicast based multicast problem. By eliminating the buffer we can significantly reduce the power.

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