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A Review Paper on Design and Simulation of Universal Asynchronous Receiver Transmitter on Field Programmable Gate Array Using VHDL

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Abstract: ***Universal Asynchronous Receiver Transmitter (UART) is the use of the serial communication protocol, low velocity, short-distance, low-cost data exchange between computer & peripherals. During the genuine industrial production, sometimes we demand to simply integrate core part rather than full functionality of the UART. UART includes three modules which are received, the baud rate generator and transmitter. The UART design with Very High Description Language can be integrated into the Field Programmable Gate Array to achieve reliable, compact & stable data transmission. It's significant for the design of System on Chip. In the result and simulation part, this project will focus on check the receive data with error free & baud rate generation at different frequencies. Likewise, in the Baud Rate Generator part, before the overall design is synthesized into the UART design the Baud Rate Generator is incorporated. The role of frequency divider here we can use this at those places where we require lower frequent to operate the functionality. This frequency divider will automatically adjust according to demand. All modules are designed using VHDL and implemented on Xilinx FPGA development board.***

Keywords: VHDL, FPGA, Xilinx ISE.

I. INTRODUCTION

In several control systems, the UART can be widely used for serial communication circuit. A universal asynchronous receiver/transmitter which plays the vital role in serial data transmission. It manages the conversion between parallel & serial data. In Serial communication, there occurs, reduction of the distortion of a signal; therefore it is possible to make data transfer between two systems at great distance. A Universal Asynchronous Receiver Transmitter includes a receiver & a transmitter. The transmitter is a distinctive shift register that loads data in parallel, then at a specific rate it shifts out bit by bit. On the other hand The receiver shifts the data bit by bit and then rearrange the data. UART transmitter controls communication by getting a data word in parallel format & directing the Universal Asynchronous Receiver Transmitter to transmit it in a serial format.

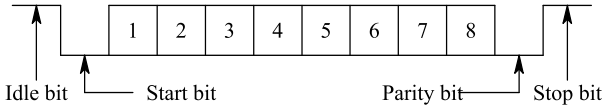

Fig. 1 UART frame format

The Receiver must detect transmission & accept the data in serial format, remove the start bits, stop bits, & store the data in a parallel format. So the UART is asynchronous in working, whenever start bit is received, the receiver generates local clock in order to synchronize to broadcast as the recipient does not recognize when the information will arrive. Asynchronous communication permits data to be sent without the transmitter having to transmit a clock signal to the receiver. This project uses Very High Description Language to implement the Universal Asynchronous Receiver Transmitter core functions & integrate them into an FPGA chip to achieve stable, compact and reliable data transmission. In this project also design different baud rate on UART for synchronization of transmitter to receiver through RS232 by using FPGA. So that it will provide various features like It is a microchip that controls a computer's an interface to its attached serial devices**,** Asynchronous serial communication has advantages of long transmission distance, less transmission line, high reliability, and the growth in communication media has resulted in a greater demand for efficient & fast serial communication.

II. RELATED WORK

Dr. Garima Bandhawarkar Wakhle et al. suggested that, the UART is the use of the serial communication protocol, which permits the full duplex communication in serial link. They design the hardware implementation of a high speed & competent UART using Field Programmable Gate Array. The UART consists of three components, namely receiver, transmitter & baud rate generator which is also frequency divider. They simulated on Modelsim SE 10.0a and design by using Verilog description language which has been synthesized on FPGA kits like as Spartan3 & Virtex4. After analyzing the comparative analysis conclude that there is a difference in between the number of slices, LUTs and the maximum frequency. The results are quite stable and reliable and have great flexibility with high integration. If we use FIFO in making the UART our design becomes more flexible, stable and reliable which provides highest bps rate. [1]

Amanpreet Kaur, Amandeep Kaur concludes that, A UART is a full duplex receiver and transmitter. It is the chip with programming that controls a computer's an interface to its connected serial devices. It manages the transmission between serial and parallel data. The whole process of serial transmission is operating on the principle of the shift register. In data transmission through the UART, once the baud-rate has been originated, both the transmitter & the receiver's internal clock are set to the identical frequency. [2]

As per Bhavna manure and Rahul tenure is concerned, developing a serial communication protocol including a bit synchronization, automatic baud rate detection with selection and bus, frequency division according to the input clock. All modules are simulated on Xilinx Spartan-3 FPGA development board using Verilog programming language and. In the simulation part focus on check the receive data with error free & baud rate generation at various frequencies. The Baud Rate Generator is incorporated into UART design, before the entire design is synthesized. The importance of frequency divider at such places where the user needs lower frequent to operate the functionality. This frequency divider will automatically adjust as per requirement. Observed simulated waveforms at various frequencies between 150 bps to 38400 bps at 50 MHz clock cycles. The simulated waveforms in this prove the consistency of the HDL implementation to describe the architecture and features of the baud rate generator with UART design. [3]

Fang Yi-yuan Chen Xue-Jun mention that Universal Asynchronous Receiver Transmitter is mainly using for serial communication as well as for low speed, short-distance, low-cost data exchange between computer and its peripherals. The UART designed with VHDL language can be consolidated into the Field Programmable Gate Array to achieve stable, compact & efficient data transmission. It's important for the design of System on Chip. The results of simulation on Quartus II are

completely reliable with the UART. In this paper for designing it uses VHDL as a design language to acquire the modules of the UART. The simulation and test part is done by using Quartus II software Altera Cyclone series FPGA chip. The results are reliable & stable, the design has high integration, great flexibility with some reference value. Mainly in electronic designing field, where SOC technology has recently become widely used, this design shows great significance. [4]

From the survey, it is observed that the implementation of UART basically uses the on-chip UART IP hard core because it has high performance, but it has poor flexibility and poor transportability, hence it is usually unable to meet the high requirements of the customer. With the rapid development of FPGA soft core plays an increasingly important role in embedded system, depending on the high performance, high flexibility, transportability and configuration. Huimei Yuan, Junyou Yang and Peipei Pan presented new methodology that provide simple Design of UART IP Soft Core based on DMA Mode. [5]

III. CONCLUSION

From review of various papers we conclude that this design uses VHDL language to acquire the modules of Universal Asynchronous Receiver Transmitter. Using the Xilinx software, FPGA chip to complete simulation and test. The results will be stable and reliable. The design will consist high integration and great flexibility with reference values. Especially in the field of electronic design technology has recently become widely used, this design shows great significance.

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