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Design and Implementation of Wireless Module using VHDL – A Review

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Abstract: Nowadays, network-on-chip (NoC) systems are becoming more popular due to their big advantages when compare with systems-on-chip (SoC). Considering the problems of multi-hop communication, transfer latency, network throughput, energy dissipation and improve the performance of a large NoC system, the idea of inserting wireless links offers a potential solution. We can be developed a hybrid mechanism to transfer data by taking the advantages of both wireless and wired communications. By using a scalable mechanism for NoCs architecture that minimizes the power consumption via hybrid wireless communication channels. In this paper, we merge both hybrid and scalable channels in order to reduce the area overhead with smaller routers and shared buffers and power consumption and improve performance by minimizing the hop count.

Keywords: Network-on-chip (NoC), Wireless network on chip (WNoC), XY Routing algorithm.

I. INTRODUCTION

If the number of components in a system is large, buses are the dominating technology for system-on-chips. However, the bus is a communication bottleneck and severe limitations like limited bandwidth and scalable up to a certain extent. These limitations are overcome in Networks-on-Chip which provide a much larger amount of communication resources and are scalable. On-chip wireless communication fulfills system feasibility and flexibility to overcome limitation of wired communication using existing and well-understood CMOS technology. To extract its wireless capabilities, multi hop NoC wired channels are replaced single-hop wireless channels with High-bandwidth so that transmission performance, power consumption and long distant communication problems of traditional wired NoC can be addressed simultaneously.

The continuing demand for high-speed interconnects with technology scaling and low-power, the on-chip wireless communication network is capable of bringing significant performance gains for multicore SoCs. Wireless NoCs (WiNoCs) can be designed by using small on-chip antennas as an enabling technology. Antennas can be used to eliminate a number of wired interconnections between the less-traveled paths of communication on the chip.

WNoC architecture is based on a conventional wired 2-D mesh NoC architecture called Network-based Processor array. Each Processing Element (PE) consists of a processor core, Network Interface and router. To increase network performance and provide fault tolerant routing ability, it utilizes an XY routing scheme. Data delivery in WNoC is done by wormhole packet switching, because it has advantages of both low transfer latency and low buffer requirement. First flit of a packet is the header

flit, which carries control information for packet delivery, such as destination address, payload size, packet type, sequential number and some control flags.

WNoC Architecture

In WNoC, we propose to divide the whole system into multiple small clusters of neighboring cores and call these smaller network subnets as shown in fig (1) called this subnetwork as internetwork and intranetwork. Inter-subnet communication will be done through the wireless links, while the intra-subnet communication is still wireline. Each subnet is with a wireless base station (WB), which is capable of transmitting and receiving data packets over the wireless channels.

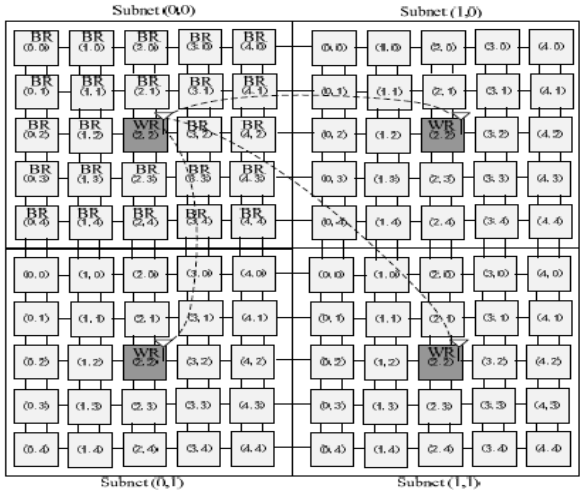

Figure 1: 10x10 WNoC Architecture

Each Processing Element (PE) consists of a processor core, Network Interface (NI) and a router as shown in Fig 2. A network interface is the point of interconnection between a computer and a private or public network. The network interface can be implemented in software. A network interface is generally a network interface card (NIC), but does not have to have a physical form.

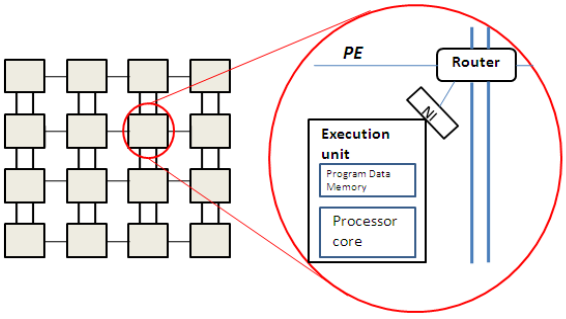

Figure 2: 4x4 2-D NePA architecture

II. Related Work

Current commercial systems-on-chips (SoCs) designs integrate large number of predesigned cores and their number is predicted to increase significantly in the near future. For example, molecular-scale computing promises multiple order-of-magnitude improvements in device densities. But the development of such kind of chips is not an easy task as the number of transistors increases on-chip and so does the complexity of integrating them. SoCs use shared or dedicated buses to interconnect the communicating on-chip resources. The bus is a communication bottleneck and also the bandwidth is limited. However, beyond a certain limit, these buses are not scalable.

In [1] Dally and Towles in 2001 proposed replacing design specific wires with general purpose, (packet-switched) network, hence marking the beginning of network-on-chip (NoC) era. Network on-Chips are emerging as an alternative communication

platform with the basic idea borrowed from computer networks for complex multi-processor SoCs The network-on-chip (NoC) is an enabling technology for integration of large numbers of embedded cores on a single die. Networks-on-Chip provides a much larger amount of communication resources and are scalable thus overcome the limitation of buses. The performance benefits of conventional Network-on-Chip (NoC) architectures are limited by the high latency and energy dissipation in long distance multihop communication between embedded cores.

In [4] V.Soteriou el.at..2009 worked on router to increase throughput of the network for NOC by adding extra crossbar and complex arbitration scheme. This architecture shows a significant improvement in throughput at the expense of area and power due to extra crossbar and complex arbitration scheme. They get up to 94% of throughput, but power consumption is increased by the factor of 1.28.

In [6] A. Louri el.at. Put the idea of inserting repeater on inter-router links with adaptive control and eliminating some of the buffers in the router. This approach saves the appreciable amount of power and latency and area without significant degradation in the throughput. But there is some scope required to increase the buffer utilization inside the router.

In [7] Ying-Cherng Lan el.at. Addresses the buffer utilization. This utilization is done by making the channels bidirectional and shows significant improvement in the system performance. But in this case, each channel controller will have two additional tasks: dynamically configuring the channel direction and to allocate the channel to one of the routers, sharing the channel. Also, there is a 40% area overhead over the typical NoC router architecture due to double crossbar design and control logic.

In [5] Neishabouri proposes Reliability Aware Virtual Router architecture in which they allocate more memory to the busy channels and less to the idle channels. This allocation of storage shows 7.1% and 3.1% latency decrease under uniform and transpose traffic patterns respectively at the expense of complex memory control logic. This solution is latency efficient but not area and power efficient.

In [3] The fundamental limitation faced by wired interconnects for the billion-transistor SoCs may not overcome by NoC. Recent advances in silicon integrated circuit technology are making possible tiny, low-cost antennae, receivers and transmitters to be integrated onto a single chip are known as Radio-on-Chip technology. As a result, M.C.F. Chang introduced an alternative RF/wireless interconnect technology for future on-chip communication. Chang in 2008 proposed a hybrid design that uses electrical wires along with an RF transmission line (shortcut) to propagate RF signals at the speed of light. This design achieved an increase in performance using low energy RF transmission line of 1.2 pJ/bit. This wire-line approach adds a slight area overhead due to the transmission line laid on the chip.

In [8] Lee in 2009 proposed a wired/wireless hybrid design called WCube which uses a centralized wireless hub at each group of 64 nodes. There is a fixed wireless link for intergroup communication and wires in intragroup communication. Each wireless hub uses a single transmitter with multiple receivers that operate in the 100-500 GHz frequency range and consume 4.5 pJ/bit. The results showed an improvement in latency while consuming a power comparable to a mesh network.

In [9] Amlan Ganguly and Kevin Chang in dec2009, elaborate the design principles for a hybrid wines and also discussed the Antenna characteristic of carbon nanotubes (CNTs) in the THz/optical frequency range. Thus, antennas operating in the THz/optical frequency range can support much higher data rates. Such nanotube antennas are good candidates for establishing on-chip wireless communications links

In [10] More recently, Ganguly 2010 proposed a scalable hybrid design using several centralized wireless hubs connected in a ring. A low energy of 0.33 pJ/bit was achieved with carbon nanotube antennas and on-chip optical modulators.

In [11] On-chip interconnects carrying signals between different blocks will be the bottleneck for system performance and reliability. To tackle this problem, Chifeng Wang in 2011 developed an on-chip communication infrastructure based on a

network-on-chip architecture and developed a hybrid mechanism to transfer data among IP cores by taking advantages of both wireless and wired communications. By using on-chip antennas hence named as WNoC (Wireless Network on Chip) which provide on-chip wireless communication to transfer data across long distances and energy dissipation and minimize transfer latency accordingly. The experimental results showed significant improvement in transfer latency, energy dissipation and network throughput. But, WNoC routers still need to consistently improve router mechanisms so as to enhance transmission quality.

In this paper, we are considering the problems of multi-hop communication, transfer latency, network throughput, and energy dissipation and improve the performance of a large NoC system; the idea of inserting wireless links offers a potential solution. We can be developed a hybrid mechanism to transfer data by taking the advantages of both wireless and wired communications. By using a scalable mechanism for NoCs architecture that minimizes the power consumption via hybrid wireless communication channels. In this paper, we merge both hybrid and scalable channels in order to reduce the area overhead with smaller routers and shared buffers and power consumption and improve performance by minimizing the hop count.

III. CONCLUSION

From the review of various papers we have concluded that NoC provides the great solution over the limitations of SoC. WNoC is designed by using miniaturized antenna provides the easy and less traffic communication between the different subnetworks. In this paper, we can be developed a hybrid mechanism to transfer data by taking the advantages of both wired and wireless communications. The advantage of wormhole packet switching is that it achieves minimum network delay and needs less buffer space also provide higher scalability, but also facilitates reuse of the communication architecture.

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