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A Review Paper on Implementation of UART Controller with Automatic Baud Rate Generator using FPGA

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Abstract: ***UART (Universal Asynchronous Receiver Transmitter) is a kind of serial communication protocol; mostly used for short-distance, low speed, low-cost data exchange between computer and an output device. In this, we present a design method of asynchronous FIFO and the structure of the controller. This controller is designed with UART circuit block and FIFO circuit block within the FPGA to implement communication in modern complex systems quickly and effectively. Here we use VHDL to implement the UART core functions and integrate them into an FPGA chip to get stable and reliable, compact data transmission. In the result and simulation part, we will focus on baud rate generation at different frequencies and check the receive data with error free. The Baud Rate Generator is incorporated into the UART design. This frequency divider will automatically adjust according to requirements. To meet modern complex control systems communication demands, we can design a multi-channel UART controller based on FIFO technique, FPGA and it is also significant for the design of SOC.***

Keywords: UART, Baud rate generator, Shift register, FIFO.

I. INTRODUCTION

Asynchronous serial communication has advantages of high reliability, less transmission line and long transmission distance, therefore is widely used to exchange data between a computer and external devices.

Asynchronous serial communication is implemented by UART. It provides full-duplex communication in serial link; this has been widely used in the data communications. UART includes a transmitter and a receiver. Transmitter controls transmission by taking a data word in parallel format and directing the UART to transmit it in a serially. Likewise, the Receiver must detect transmission, receive the data in serially, and store the data word in a parallel format. The conversion of serial to parallel data is handled by UART. Serial communication reduces the distortion of a signal; therefore data transfer is possible between two systems separated by great distance. The UART serial module is divided into three sub-modules: the baud rate generator, receiver module and transmitter module. The baud rate generator is used to produce a local clock signal. In data transmission through the UART, once the baud-rate has been established, both the transmitter and the receiver's internal clock are set to the same frequency. TXD is the transmit side, i.e. the output of the UART; RXD is the receiver, i.e. the input of the

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UART. The UART receiver module is used to receive the serial signals at RXD and convert them into parallel data. The UART transmit module converts the data bytes into serial bits according to the frame format and transmits those bits through TXD.

UART's basic features are: There are two states in the signal line, using logic high and logic low to distinguish respectively. UART frame format consist of a start bit, data bit, parity bit and stop bit. After the Start Bit the data bits are sent, with the Least Significant Bit (LSB) sent first. The start bit is always low and the stop bit is always high. When the complete data word has been sent, it adds a parity bit this parity bit may be used by the receiver to perform error checking. Then at least one Stop Bit is sent by the transmitter. Because asynchronous data are "self-synchronizing", if there is no data to transmit, the transmission line will be idle. The UART frame format is shown below

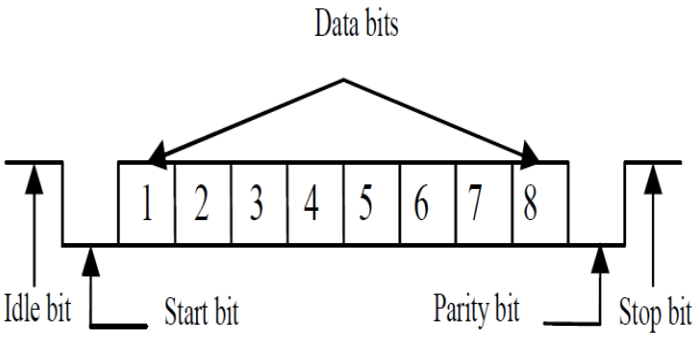
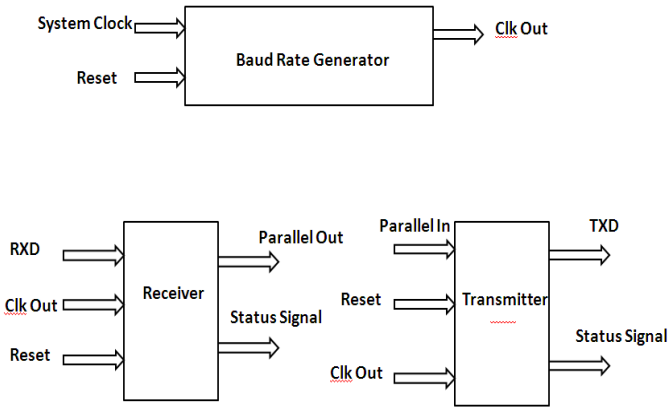


Figure 1. UART Frame Format

Basic Diagram of UART



Baud Rate Generator

Baud Rate Generator is actually a kind of frequency divider. The baud rate, frequency factor can be calculated according to a given system clock frequency and the required baud rate. Then the baud rate, frequency factor, calculated is used as the dividing factor.

Let the system clock is 50MHz, baud rate is 9600bps, and then the output clock frequency of the baud rate generator should be 1* 9600Hz. Therefore the frequency coefficient (M) i.e. counts the value of the baud rate generator is

$$M = 50MHz/1*9600Hz$$

$$M=5208$$

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II. Related Work

FANG Yi-Yuan CHEN XUE- Jun has presented a paper on "Design and simulation Of UART serial communication Module Based on VHDL". In this paper they presented that the UART is the microchip with programming that controls a computer's interface to its peripherals. It is the most widely used serial data communication circuit ever. The whole process of serial transmission is based upon the principle of the shift register. There are two primary forms of serial transmission that are Synchronous & Asynchronous. In Synchronous serial communication requires that the sender and receiver should work on the same clock with one another. Asynchronous transmission allows data to be transmitted without sending a clock signal to the receiver. This design uses VHDL as the design language to achieve the modules of the UART. The results are reliable & stable. The design has high integration, great flexibility with some reference value [1].

Shouqian Yu, Lili Yi, Weihai Chen, Zhao Jin Wen presented a paper on "Implementation of a Multi-channel UART Controller Based on FIFO Technique and FPGA". In this paper they have presented that in several systems such as high data collection system, a high speed control system based on PCI and multi-DSP signal processing system, FIFO is used for complete communication between high speed device and low speed device or to complete communication between the same sub controllers. FIFO is the most important part of these systems and it works as a bridge between different devices. At the same, in our controller, asynchronous FIFO based on FPGA is also the most important part. So the features and capabilities of the asynchronous FIFO determine the features of our controller. The FIFO can be used to complete communication in parallel or serial port [2].

Bhavana Mahure and Rahul Tanwar have presented a paper on "UART with automatic baud rate generator and frequency divider". In this paper they have presented that the most commonly used numbers of data bits of a serial connection are eight, which corresponds to a byte. When a regular ASCII code is used in communication, only seven LSBs are used and the MSB is 0. If the UART is configured as 8 data bits, 1 stop bit, and no parity bit, the received word is in the form of 0-dddd-ddd-0-1, in which d is a data bit and can be 0 or 1. Assume that the UART configuration is 8 data bits, 1 stop bit, and no parity bit, and the baud rate can be 4800, 9600, or 19,200 baud [3].

The circuit produces Frequency Division as it now divides the input frequency by a factor of two. Frequency Divider is dividing the frequency according to system requirement. So we can use this UART with frequency divider, no need to attach another device in that system to divide the frequency.

Nurul Fatihah Jusoh, Azlina Ibrahim, Muhamad Adib Haron and Fuziah Sulaiman presented a paper on "An FPGA Implementation of Shift Converter Block Technique on FIFO for UART" the paper represents the implementation of the bidirectional shift converter technique with FIFO circuit block and UART circuit block through FPGA device using Verilog HDL language to be applied in embedded system converter RS232 to USB (Universal serial bus) [4].

Nennie Farina Mahat presented a paper on " Design of a 9-bit UART Module Based on Verilog HDL." In this paper, a modified UART design is proposed with automatic address indicated, which is called 9-bit UART [5]

"Platform-Independent Customizable UART Soft-Core" Biplab Roy. In this paper, we propose a technique for software implementation of a UART using shift register with the goal of getting a customizable UART-core which can be used as a module in implementing a bigger system irrespective of one's choice of the implementation platform [6].

"An Adaptable UART Based Configuration and Read-out Interface for IC Prototypes" Jan Henning Mueller, Mojdeh Hamzavi Nejad Moghaddam, Bastian Mohr, Sebastian Strache, Ralf Wunderlich and Stefan Heinen. In this paper for PCs without a serial interface, USB can be used. The universal protocol is implemented in a hardware description language (HDL) on the IC side and in MATLAB on the PC side and can be easily adapted to the requirements and the structure of the specific IC. [7]

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Here we use VHDL to implement the UART general functionality. The transmission and reception of the various data frames are tested and verified with the modeling of a UART protocol controller. Using a hardware description language allows us to describe the function of the transmitter in a more behavioral manner, rather than focus on its actual implementation at the gate level. The simulated waveforms in this paper have proven the reliability of the HDL implementation to describe the characteristics and the architecture of the design UART with baud rate generator.

III. CONCLUSION

From the review of various papers we have concluded that the authors had used FIFO and Shift register separately for storing the data and in some paper they have used baud rate generator with single frequency. In this we had used FIFO as well as Shift register and also an automatic baud rate generator which will change its baud rate according to the change in frequency. This design uses VHDL language to achieve the modules of the UART. Software Xilinx and modelsim are used for synthesis and simulation purpose. In this paper, interfacing of PCs with FPGA using serial cable, to access the data from PC hyper terminal in FPGA at a multiple baud rate.

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